A

Major Project Report on

EVALUATING SRAM CELL PERFORMANCE AT 22NM: COMPARATIVE ANALYSIS OF 6T,7T,8T AND 9T TOPOLOGIES

Submitted in partial fulfillment of the requirement for the award of degree of

BACHELOR OF TECHNOLOGY
IN

ELECTRONICS AND COMMUNICATION ENGINEERING

SUBMITTED BY

L.AKILESH	**218R1A0433**
M.AGNI	**218R1A0434**
M.SAMPATH	**218R1A0435**
M.VINAY KUMAR	**218R1A0436**

Under the Esteemed Guidance of

Mr. VASSEM AHMED QURESHI
Associate Professor

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CMR ENGINEERING COLLEGE

UGC AUTONOMOUS

(Approved by AICTE, Affiliated to JNTU Hyderabad, Accredited by NBA & NAAC)
Kandlakoya (V), Medchal (M), Telangana – 501401

2024-2025

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that the Major Project work entitled "**EVALUATING SRAM CELL PERFORMANCE AT 22NM: COMPARATIVE ANALYSIS OF 6T,7T,8T AND 9T TOPOLOGIES**" is being submitted by **L. AKILESH** bearing Roll No: **218R1A0433**, **M. AGNI** bearing Roll No**: 218R1A0434**, **M. SAMPATH** bearing Roll No:**218R1A0435**, **M. VINAY KUMAR** bearing Roll No: **218R1A0436** in B. Tech IV-II semester, Electronics and Communication Engineering is a record Bonafide work carried out by then during the academic year 2024-25.

INTERNAL GUIDE

Mr. VASSEM AHMED QURESHI

Associate Professor

HEAD OF THE DEPARTMENT

Dr. SUMAN MISHRA

Professor

EXTERNAL EXAMINER

ACKNOWLEDGEMENTS

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DECLARATION

We hereby declare that the project work entitled "**EVALUATING SRAM CELL PERFORMANCE AT 22NM: COMPARATIVE ANALYSIS OF 6T,7T,8T AND 9T-TOPOLOGIES**" is the work done by us in campus at **CMR ENGINEERING COLLEGE**, Kandla Koya during the academic year 2024-2025 and is submitted as Major project in partial fulfillment of the requirements for the award of degree of **BACHELOR OF TECHNOLOGY** in **ELECTRONICS AND COMMUNICATION ENGINEERING FROM JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD**.

L.AKILESH	**218R1A0433**
M.AGNI	**218R1A0434**
M.SAMPATH	**218R1A0435**
M.VINAY KUMAR	**218R1A0436**

CONTENTS

ABSTRACT

As semiconductor technology advances into the 22nm node, the performance and stability of Static Random Access Memory (SRAM) cells become increasingly critical for maintaining efficient and reliable operation in modern integrated circuits. This study provides a comparative analysis of various SRAM cell topologies, specifically 6T, 7T, 8T, and 9T configurations, at the 22nm technology node. The evaluation focuses on key performance metrics including read/write stability, power consumption, noise margins, and area efficiency.

The 6T SRAM cell, while traditional and widely used, faces challenges in stability and read/write performance due to scaling effects. The 7T SRAM cell introduces an additional transistor to improve stability at the cost of increased area. The 8T SRAM cell further enhances stability and read margin by isolating the read and write paths, though it results in higher area and power consumption. The 9T SRAM cell provides additional improvements in stability and noise margins, offering a balanced trade-off between performance and area.

The relentless scaling down of CMOS technology has brought significant challenges to Static Random-Access Memory (SRAM) design, particularly in terms of stability, power consumption, and performance. This study presents a comparative analysis of SRAM cells with 6-transistor (6T), 7-transistor (7T), 8-transistor (8T), and 9-transistor (9T) topologies at the 22nm technology node. The evaluation focuses on key performance metrics, including

Read and write stability, static noise margin (SNM), power dissipation, and area overhead. The traditional 6T SRAM cell, while being the most commonly used due to its simplicity and lower area, faces significant issues related to stability and leakage current at the 22nm technology node. To address these issues, alternative topologies such as 7T, 8T, and 9T have been proposed, each adding transistors to enhance stability and reduce leakage.

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CHAPTER 1

INTRODUCTION

Static Random-Access Memory (SRAM) plays a crucial role in modern computing systems, particularly in high-speed cache memories. As technology scales down to the 22nm node, designing energy-efficient and stable SRAM cells becomes increasingly challenging due to variability effects, leakage currents, and reduced noise margins. This study presents a comparative analysis of 6T, 7T, 8T, and 9T SRAM cell topologies at the 22nm technology node, evaluating their performance in terms of power consumption, stability, and speed.

The traditional 6T SRAM cell remains the most widely used design due to its compactness and balanced read/write performance. However, it suffers from read stability issues and higher leakage power, making it less suitable for ultra-low-power applications. Alternative topologies, such as 7T, 8T, and 9T SRAM cells, have been developed to improve read stability, write ability, and leakage control. The 7T cell introduces a decoupled read path, enhancing read stability without significantly increasing area overhead. The 8T SRAM further isolates the read and write operations, leading to better noise margins and reduced power consumption. The 9T SRAM cell provides additional enhancements in read stability and leakage reduction, making it ideal for low-power and high-reliability applications.

1.1 OVERVIEW OF THE PROJECT

This project focuses on evaluating the performance of different SRAM cell topologies— 6T, 7T, 8T, and 9T—at the 22nm technology node, with an emphasis on comparing key performance metrics such as stability, read and write access time, power consumption, area efficiency, and noise margins. As the semiconductor industry continues to push towards smaller technology nodes, particularly 22nm, SRAM cells play a pivotal role in providing high-speed, low-power data storage for a variety of applications in microprocessors, memory systems, and embedded devices. However, as transistor sizes shrink, challenges such as reduced noise margins, process variations, and increased leakage currents become more pronounced. While the 6T SRAM cell is the standard due to its balanced trade-off between speed, area, and power consumption, alternative topologies like the 7T, 8T, and 9T configurations have been proposed to address these emerging issues. These topologies typically offer improvements in stability, power efficiency, and read/write performance at the cost of increased complexity and area overhead.

To carry out the analysis, the project utilizes SPICE-based simulations using standard Electronic Design Automation (EDA) tools, such as Cadence or Synopsys, to model and simulate each SRAM topology at the 22nm technology node. These simulations will provide detailed insights into the electrical characteristics, including access times, stability margins, and power dissipation, for each configuration. The results will be compared across all topologies, taking into account the impact of process variations on each design's robustness. Through this evaluation, the project aims to deliver a comprehensive understanding of how different SRAM topologies perform at advanced nodes, and it will provide recommendations on the optimal configuration for various application requirements, such as low-power devices or high-performance processors.

By exploring the strengths and weaknesses of the 6T, 7T, 8T, and 9T SRAM cells at the 22nm node, the project seeks to offer valuable insights into the trade-offs between power, performance, and area. The findings are expected to contribute to the ongoing efforts in designing more efficient, reliable, and robust memory systems for next-generation integrated circuits and computing devices.

1.2 OBJECTIVE OF THE PROJECT

The primary objective of this project is to conduct a comprehensive evaluation of the performance of different SRAM cell topologies—6T, 7T, 8T, and 9T—at the 22nm technology node. As semiconductor technology continues to scale down, traditional SRAM cells face increasing challenges related to power consumption, stability, and performance. The goal of this project is to compare these four SRAM architectures across various key performance metrics, including read/write access time, stability margins, power consumption, and area efficiency, to determine which topology offers the best trade-offs for advanced integrated circuit designs.

One specific objective is to assess the stability and noise margins of each SRAM cell configuration. As transistor sizes shrink to smaller nodes like 22nm, noise margins—critical for reliable memory operation—become increasingly susceptible to process variations, thermal fluctuations, and supply voltage fluctuations. Therefore, the project aims to understand how the stability of the 6T, 7T, 8T, and 9T SRAM cells holds up in such conditions and which configuration provides the most robust performance.

The project also aims to evaluate the impact of different SRAM configurations on area efficiency. As chip area becomes a valuable resource in advanced technology nodes, the area overhead introduced by each SRAM topology must be carefully assessed. The objective is to determine how the additional transistors in the 7T, 8T, and 9T configurations affect the overall area of the memory cell compared to the traditional 6T SRAM cell and whether the performance benefits justify the area trade-offs. This analysis will be crucial for applications that prioritize compact designs or require large memory arrays.

Finally, the project seeks to provide a detailed performance comparison of the read and write access times of the various SRAM topologies. Access speed is a critical factor for many high-performance applications, and understanding how each topology performs under typical read and write conditions at 22nm will help identify the most efficient SRAM configuration for specific use cases. By considering all these objectives—stability, power consumption, area efficiency, and access speed—the project aims to offer a comprehensive view of the advantages and trade-offs of 6T, 7T, 8T, and 9T SRAM cells at the 22nm node, ultimately providing guidance on selecting the optimal SRAM topology for future integrated circuits and memory systems.

CHAPTER 2

LITERATURE SURVEY

1. M G Srinivasa and Bhavana M S, Trans., "Performance Analysis of 6T, 8T and 10T SRAM Cell in 45nm Technology", *IJEAT*, vol. 13, no. 5, pp. 12–16, Jun. 2024.

This project focused on the design and analysis of Static Random-Access Memory (SRAM) cells, specifically the 6T, 8T, and 10T SRAM cells, for low-power applications in modern System-on-Chip (SOC) designs. As portable, battery-powered devices become increasingly prevalent, there is a growing demand for efficient power management in integrated circuits (ICs). SRAM is widely used in these devices due to its important role in providing fast, reliable memory. In particular, its substantial footprint in modern SOCs makes its design and optimization crucial for minimizing power consumption while maintaining high performance.

The project investigates the power consumption and delay characteristics of different SRAM cell designs, which are essential factors in determining the overall efficiency of memory in an SOC. The three SRAM cells studied in this work are based on the 6-transistor (6T), 8-transistor (8T), and 10-transistor (10T) configurations. Each of these designs has unique characteristics that can affect the performance in terms of power usage and speed, which are important metrics for low-power devices.

The work uses 45nm CMOS (complementary metal-oxide-semiconductor) technology for the SRAM design. This technology is known for balancing power efficiency with high- performance capabilities, making it suitable for modern electronic devices. The simulations for the 6T, 8T, and 10T SRAM cells are conducted using Cadence Virtuoso software, a widely used platform for designing and simulating integrated circuits. Cadence Virtuoso helps in creating the schematic diagrams of the SRAM cells and laying them out on the chip.

Furthermore, the project employs the ASSURA library for verification purposes. This includes performing Design Rule Checks (DRC) to ensure that the layout follows the necessary design rules, and Layout Versus Schematic (LVS) checks to verify that the physical layout of the SRAM cells matches the schematic diagram. The design operates with a low supply voltage of 1V, which is a typical approach for low-power applications.

The results of the simulations reveal that the 10T SRAM cell provides better efficiency than the 6T and 8T SRAM designs in terms of both read and write delay and power consumption. This suggests that the 10T SRAM cell is a promising candidate for applications requiring efficient low-power memory with minimized delay.

In summary, this project project presents a comparative analysis of SRAM cell designs (6T, 8T, and 10T) using advanced simulation tools to evaluate their power consumption and delay characteristics. The findings indicate that the 10T SRAM cell outperforms the other configurations, making it an effective choice for modern low-power applications.

2. Manish Verma, Shubham Yadav and Manish Kurre, "Comparitive analysis of SRAM cell topologies at 65nm technology," International Research Journal of Engineering and Technology (IRJET), 2018

This project focused on optimizing SRAM cell design for low-power applications in modern System-on-Chip (SOC) systems. SRAM cells are essential components for enabling high-performance operation of processors, and they occupy a significant portion of the area—approximately 70%—in embedded microprocessors, consuming a large part of the overall power budget. As a result, designing SRAMs that are both dense and energy- efficient, particularly in terms of reducing leakage power, is a key focus for SRAM designers.

The project compares the performance of 4-transistor (4T) SRAM cells with the conventional 6-transistor (6T) SRAM cells, using 65nm Low Standby Power (LSTP) technology. The findings reveal that iso-stable 4T SRAM cells are 10-25% denser than the conventional 6T cells, meaning that the same memory can be stored in a smaller area, reducing the overall chip size. Additionally, the 4T cells demonstrate up to 65% lower leakage power compared to the 6T SRAM cells. These improvements in density and leakage are highly beneficial for reducing the overall power consumption of the chip, making it more efficient.

However, there is a trade-off for these improvements. The 4T SRAM cells experience a 20% decrease in speed compared to the 6T cells. This speed loss is considered an acceptable trade-off, particularly for higher-level caches that require multi-cycle access. In such caches, the reduced speed does not significantly impact performance, as the system can tolerate multiple cycles for accessing data.

The project uses 65nm Low Standby Power (LSTP) technology, which is designed to minimize power consumption during idle periods, further enhancing the energy efficiency of the SRAM cells.

The results suggest that the 4T SRAM cells are a promising option for SOC designs that prioritize power efficiency and space savings, especially in applications like embedded processors or high-level caches where the speed reduction is manageable. In summary, project presents a comparison of 4T and 6T SRAM cells using advanced simulation tools to evaluate their density, leakage power, and speed. The findings indicate that the 4T SRAM cells offer significant advantages in terms of density and leakage power, making them an attractive option for low-power, area-efficient applications, with an acceptable trade-off in terms of speed.

3. Grover et al., "A 32 kb 0.35–1.2 v 50 MHz–2.5 ghz bit-interleaved sram with 8 t sram cell and data dependent write assist in 28-nm utbbfdsoi cmos", *IEEE Transactions on Circuits and Systems I: Regular Projects*, vol. 64, pp. 2438-2447, Sep. 2017.

This project presents an optimized co-design of SRAM cells, assist schemes, and layout to enable wide voltage range operation of SRAM, spanning from 0.35V to 1.2V, across all process corners. Achieving low-voltage operation in SRAM is critical for low-power applications, and this work introduces several innovative techniques to enhance the performance and reliability of SRAM cells under varying voltage conditions.

The project proposes a differential read asymmetric 8-transistor (8T) SRAM cell design, which improves the read stability and helps in operating the memory at lower voltages. Additionally, a data-dependent differential supply and body modulation write assist scheme is introduced to aid in achieving reliable write operations at reduced voltages. This write assist scheme ensures that the SRAM can function at a lower write voltage without compromising data integrity.

The project also introduces an optimized layout design that reduces the metal capacitance of the wordlines by 54%, which contributes to lower power consumption and improved performance. Furthermore, this layout enables bit-interleaving, which enhances memory access efficiency by distributing data across different memory cells.

The proposed assist scheme can be combined with conventional assist techniques to further reduce the minimum write operational voltage of the SRAM by 70-130mV, while maintaining iso-performance (the same performance level). This results in lower power consumption without causing reliability issues.

To validate the proposed design, a 32-kilobit (kb) SRAM instance is fabricated using 28-nm Ultra-Thin Body and Buried Oxide (UTBB) Fully Depleted Silicon On Insulator (FDSOI) technology, which is known for its low power consumption and high efficiency.

The efficiency of the proposed scheme is demonstrated by achieving the lowest write voltage of 0.32V, significantly lower than conventional SRAM designs. In addition, multiple read assist schemes are employed to lower the read voltage to 0.35V, enabling efficient reading at low supply voltages. The performance of the SRAM is further validated by integrating it into a Digital Signal Processor (DSP) with a measured operating frequency of 50 MHz at 0.358V, demonstrating stable operation under extremely low voltage conditions.

Finally, the project defines low-voltage and wide voltage range figures of merit to benchmark the proposed solutions against other works in the field. The results show that the proposed SRAM design, with its optimized assist schemes and layout, achieves significant improvements in low-voltage operation, making it suitable for energy-efficient, wide-voltage-range applications.

In summary, this project proposes an innovative co-design approach for SRAM cells, assist schemes, and layout optimization that enables wide voltage range operation and low-power consumption, validated through the fabrication and integration of a 32 kb SRAM instance in 28-nm UTBB-FDSOI technology.

4. Singh, S., Arora, N., and Singh, B. P., "Simulation and Analysis of SRAM Cell Structures at 40nm Technology", International Journal of Modern Engineering Project, Vol.1, No.2, pp. 327-331.

This abstract outline a project that focuses on the simulation and comparative analysis of various SRAM cell designs, with an emphasis on key parameters like power supply voltage, operating frequency, temperature stability, and area efficiency. SRAM (Static Random Access Memory) is a widely used embedded memory in CMOS ICs (Complementary Metal-Oxide-Semiconductor Integrated Circuits), and it operates using bistable latching

circuitry to store a bit of data. Due to its high-speed performance, low access time, and ability to retain data as long as power is supplied, SRAM is an essential component in many digital systems, including microprocessors, cache memories, and embedded systems.

The main goal of this project is to explore and compare the performance of different SRAM cell designs under varying conditions to assess their suitability for specific applications.

Power supply voltage impacts the overall power consumption of the SRAM cell, which is particularly important in battery-powered devices and low-power applications. Operating frequency is another important factor that affects how quickly data can be read or written to the memory. The ability of SRAM cells to perform reliably under varying temperature conditions is also evaluated, as temperature fluctuations can affect the stability and performance of the memory.

Additionally, area efficiency is a key consideration since SRAM cells occupy a significant amount of space in integrated circuits, and optimizing the area can help in designing more compact and efficient systems.

To conduct the analysis, all simulations were performed using BSIM 3V3 40nm technology, a well-established semiconductor process that provides accurate modeling for CMOS-based designs. Tanner EDA, an electronic design automation (EDA) tool, was usedfor simulating the behavior and performance of the SRAM cells. Tanner EDA is widely used in academic and industrial project due to its user-friendly interface and powerful simulation capabilities, making it an ideal tool for this study. The simulations involve different SRAM cell designs, which are compared in terms of their performance under various operational conditions.

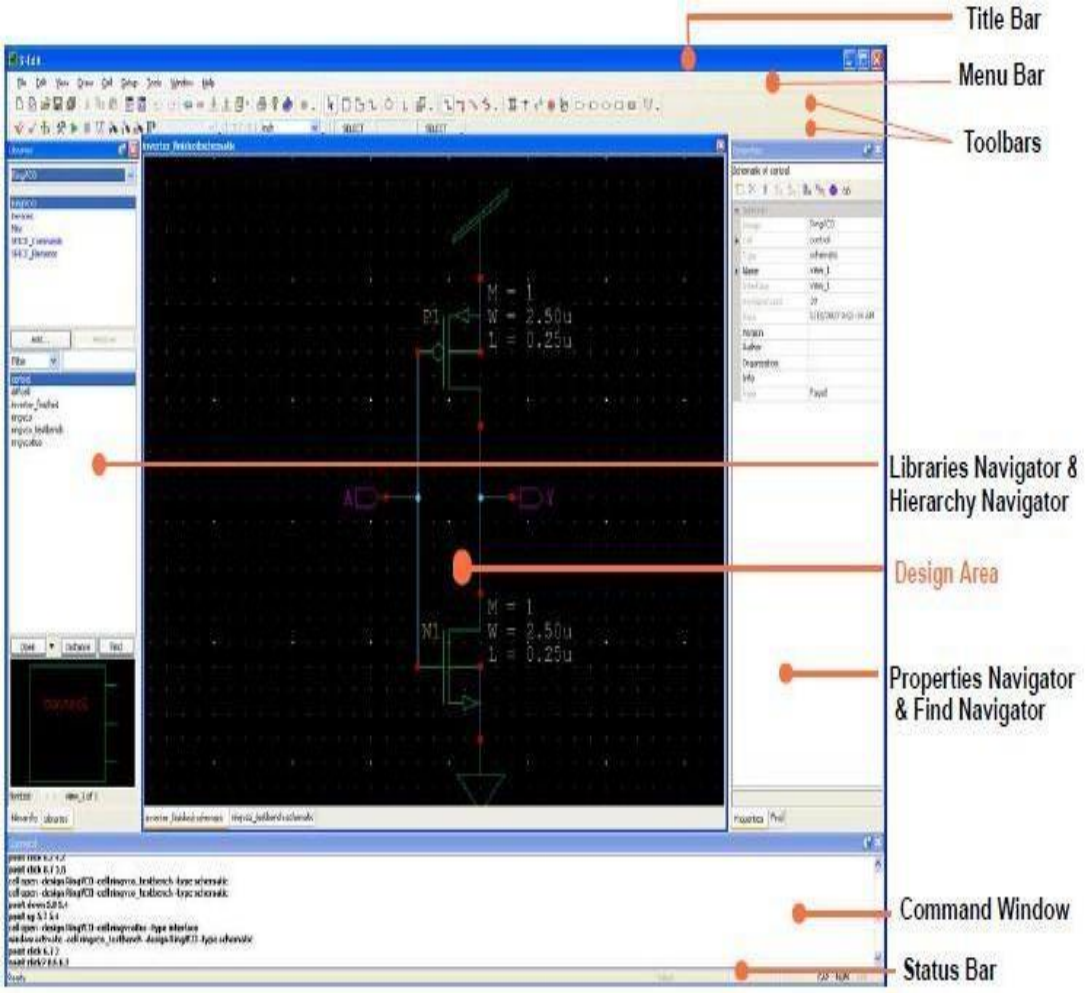
The results of this project aim to provide a better understanding of the trade-offs between different SRAM cell designs. The comparative analysis can help engineers and designers choose the most suitable SRAM cell for a particular application, taking into account factors like power consumption, speed, temperature tolerance, and area requirements. This study contributes to the ongoing development of more efficient, high-performance memory systems for CMOS ICs, particularly in low-power and compact designs.

CHAPTER 3

SOFTWARE REQUIREMENT

3.1 TANNER TOOL

Tanner EDA is a widely used Electronic Design Automation (EDA) tool for designing, simulating, and verifying analog, digital, and mixed-signal circuits. It is primarily used for integrated circuit (IC) and Very Large Scale Integration (VLSI) design. Tanner EDA provides a complete suite of tools for schematic capture, circuit simulation, layout design, and verification, making it a popular choice for students, researchers, and engineers working in ASIC, MEMS, and mixed-signal IC design.



The user interface consists of the elements shown below. Unless you explicitly retrieve a setup file, the position, docking status and other display characteristics are saved with a design and will be restored when the design is loaded.

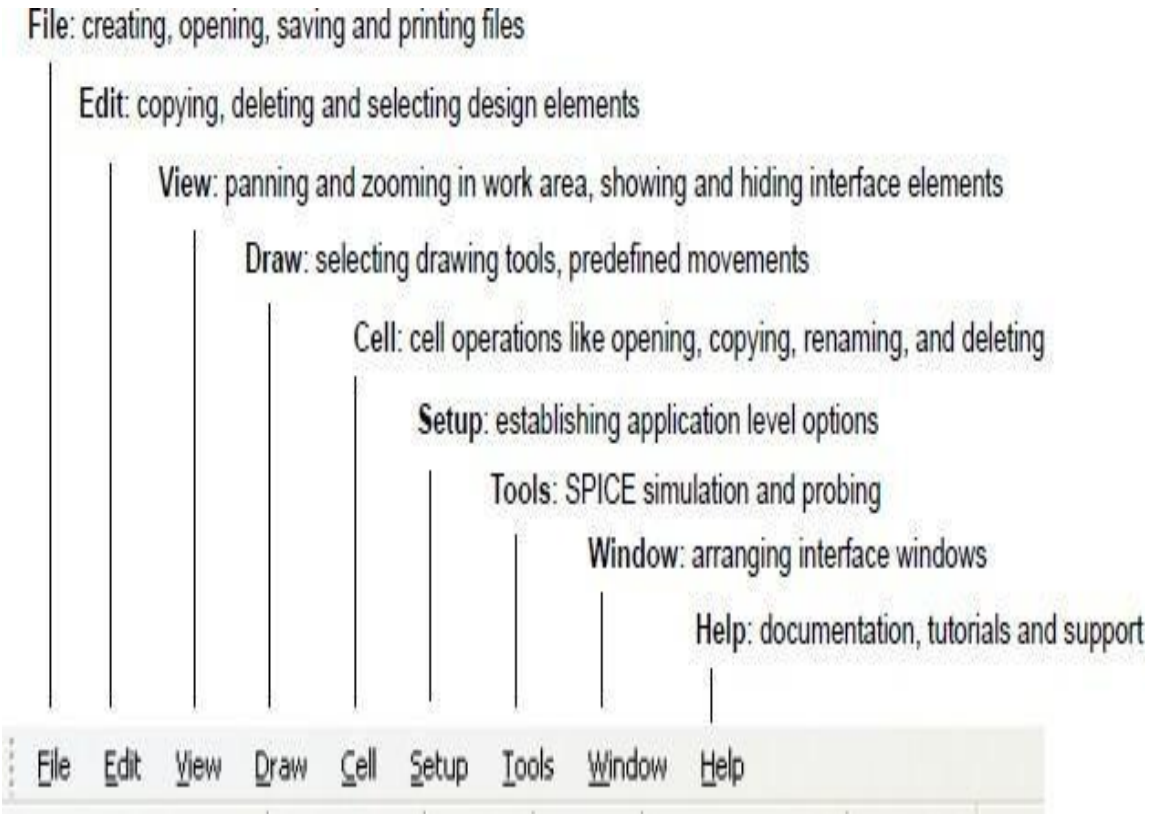
Parts of the User Interface

Title Bar

The title bar shows the name of the current cell and the view type (symbol, schematic, etc.).

Menu Bar

The menu bar contains the S-Edit menu titles. The menu displayed may vary depending on the view type that is active. See “Shortcuts for Cell and View Commands” on page 70 for the various methods S-Edit provides for executing commands.



Menu List Filtering

Most S-Edit menus and dialogs allow for filtering to speed the process of selecting from a drop- down list. So, when you enter a character, S-Edit will jump to the first list item that begins with that character. For example, typing **g** highlights the first list item beginning with that letter and filters the display to show only items that begin with **g**. Typing a **u** after the **g** highlights the first list item beginning with **gu**, and filters the display to show only items that begin with **gu**, and so on. The search procedure is case-insensitive.

Toolbars

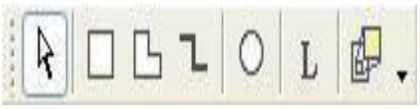
You can display or hide individual toolbars using the **View > Toolbars** command, or by right- clicking in the toolbar region. Toolbars can be relocated and docked as you like. For added convenience, S-Edit displays a tool tip when the cursor hovers over an icon.

Standard Toolbar

The Standard toolbar provides buttons for commonly used file and editing commands, as well as operations specific to S-Edit such as “View Symbol.”

Draw Toolbar

The Draw toolbar provides tools used to create non-electrical objects, such as rectangles, circles, and lines, for illustrating and documenting a design.

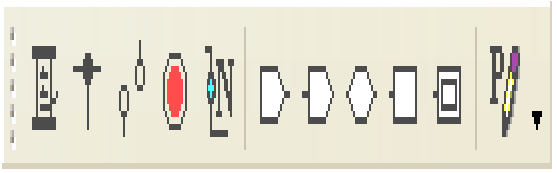


Segment Toolbar

The Segment toolbar provides tools with which you limit the degree of angular freedom allowed when you are drawing wires.

Electrical Toolbar

The Electrical toolbar provides the tools used to create wires, nets, and ports, and to add properties.

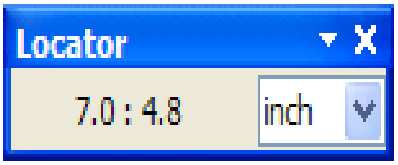


SPICE Simulation Toolbar

The SPICE Simulation toolbar lets you extract connectivity, select and probe nets, launch T- Spice and select evaluated properties.

Locator Toolbar

The Locator toolbar displays the coordinates of the mouse cursor and allows you to quickly change the units of measurement application-wide.



Mouse Buttons Toolbar

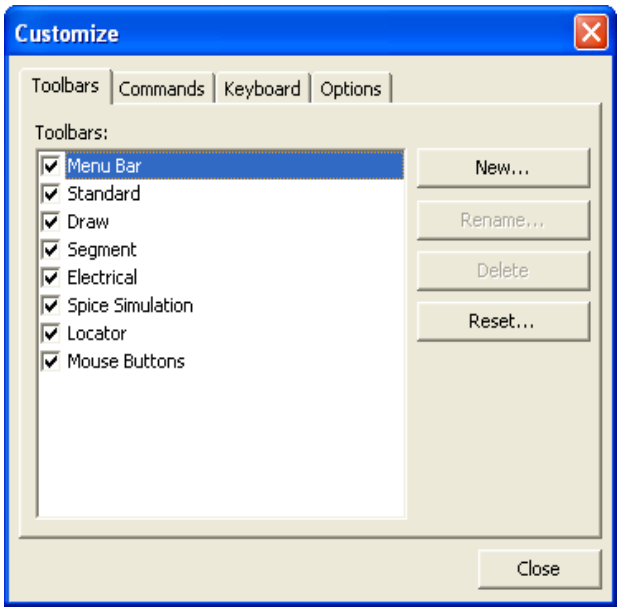
The Mouse Buttons toolbar shows the current functions of the mouse buttons.

Mouse buttons vary in function according to the tool that is active. The **Shift**, **Ctrl** and **Alt** keys can further change the function. For two-button mice, the middle-button function is accessed by clicking the left and right buttons at the same time, or by pressing **Alt** while clicking the left mouse button.

Customizing Toolbars

You can add buttons for existing commands to existing S-Edit toolbars, add entirely new toolbars, and add new buttons for entirely new commands to either new or existing toolbars. To customize toolbars, right-click anywhere in the toolbar area and click on **Customize** in the Context-sensitive menu.

This opens the **Customize** dialog, to the **Toolbars** tab. Note that in this dialog the checkmarks control only whether or not a toolbar is displayed. The buttons apply only to the toolbar that is highlighted, and will be applied even if a toolbar is not currently displayed. All toolbars are checked, so all are displayed. Only Menu Bar is highlighted, so any of the button actions (ex. Reset) will act only on the Menu Bar.

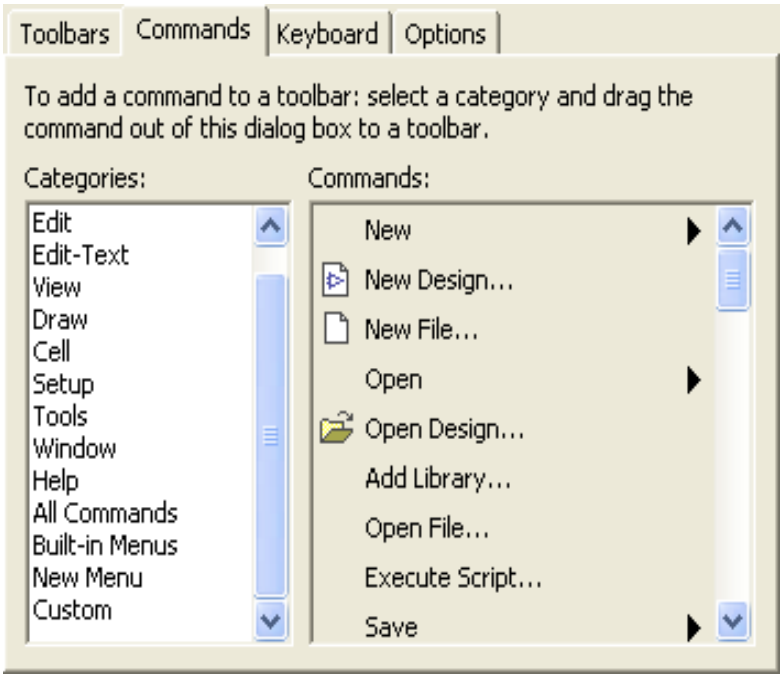


Reset returns an existing toolbar to the default display settings for aspects such as icon size, tooltips, etc.– and its original button contents.

The **New**, **Rename** and **Delete** functions apply only to custom toolbars

Adding a Command to a Toolbar

Use the Commands tab to add a button for an existing command to any toolbar.



- Right-click in the toolbar area, select **Customize** and then the **Commands** tab.
- Pick the desired command from the **Categories** list (or use All Commands for a complete list of available commands), then simply click-and-drag the command from the right column to the desired toolbar.
- S-Edit will insert a button displaying the command text, or an icon if one is already defined.

Adding a New Menu

- You can also use the **Commands** tab to add a new menu category to the menu bar.
- In the Commands tab, scroll down to **New Menu** at the end of the **Categories** list.
- Click-and-drag **New Menu** from the right column to the Menu bar in the interface.

- Right-click on the New Menu button you have just placed to open the control menu, where you can rename it, then check Begin a Group to populate the menu with pull-down commands.

- Select the new menu button in the interface to open the pull-down group, then click-and-drag from the Commands tab to add the desired command(s). Make sure to drop the commands within the group area.

3.2 Schematic design of Inverter

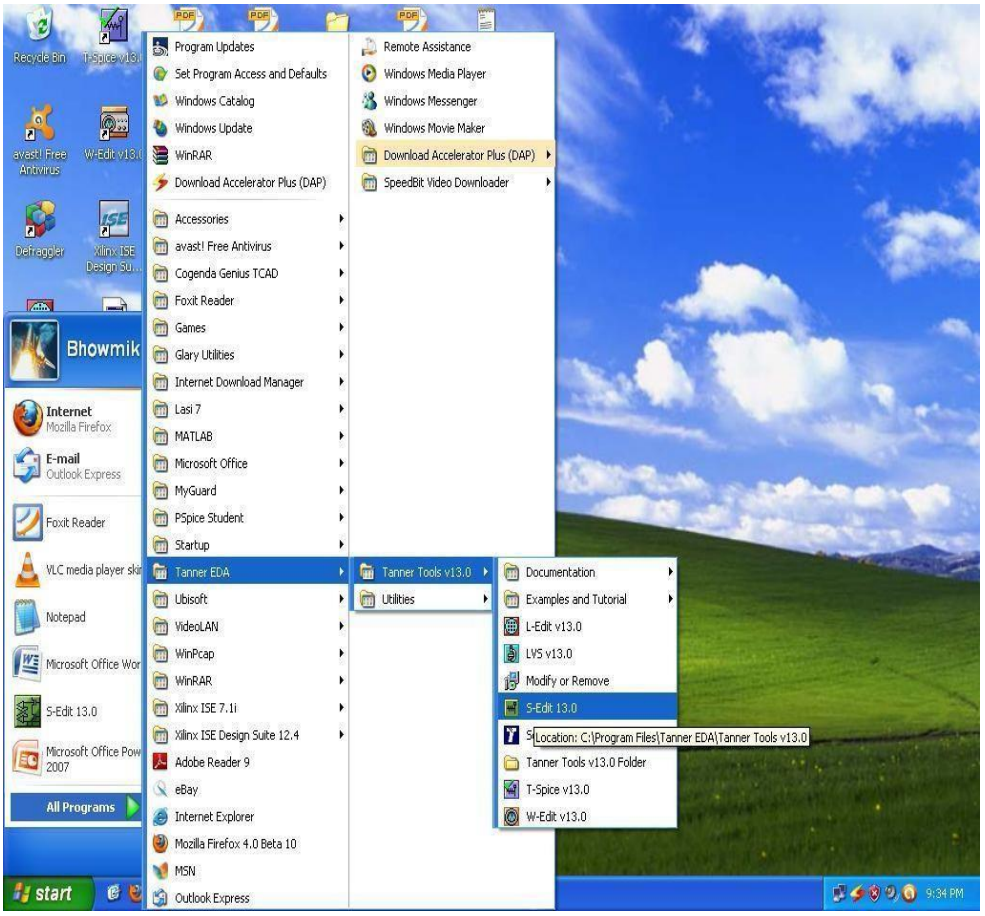
What is schematic Design: There are many phases or progressions of a design. A common term you will hear when working with a Designer is “Schematic Design”. This phase is early in the design process. Schematic Design establishes the general scope, conceptual ideas, the scale and relationship of the various program elements. The primary objective of schematic design is to arrive at a clearly defined feasible concept based on the most promising design solutions.

Opening S-edit platform:

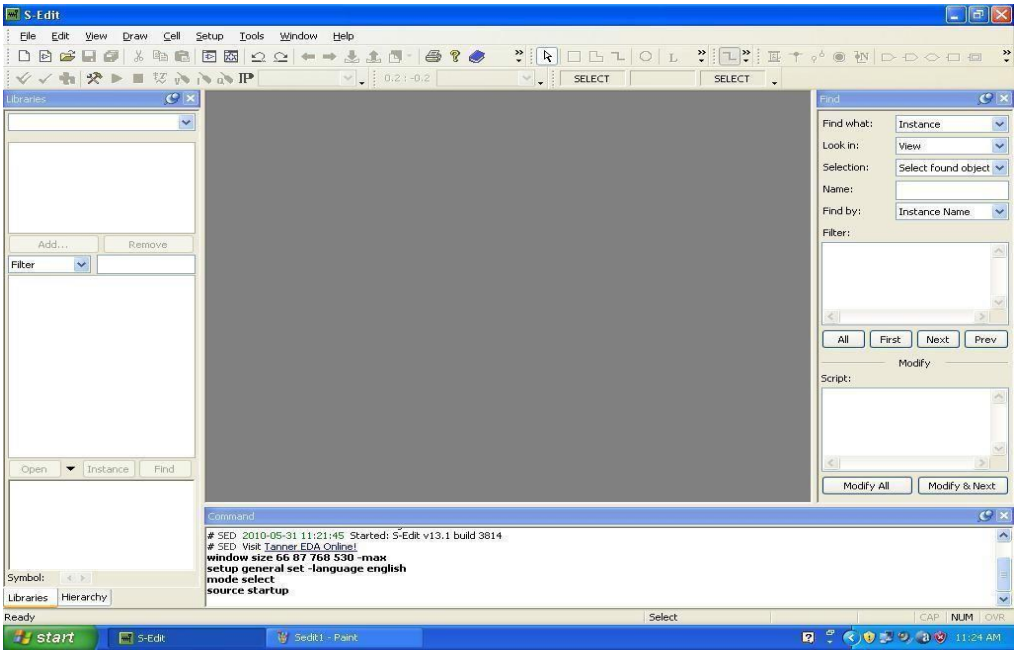
First of all double click on the icon of s-edit on the desktop

or

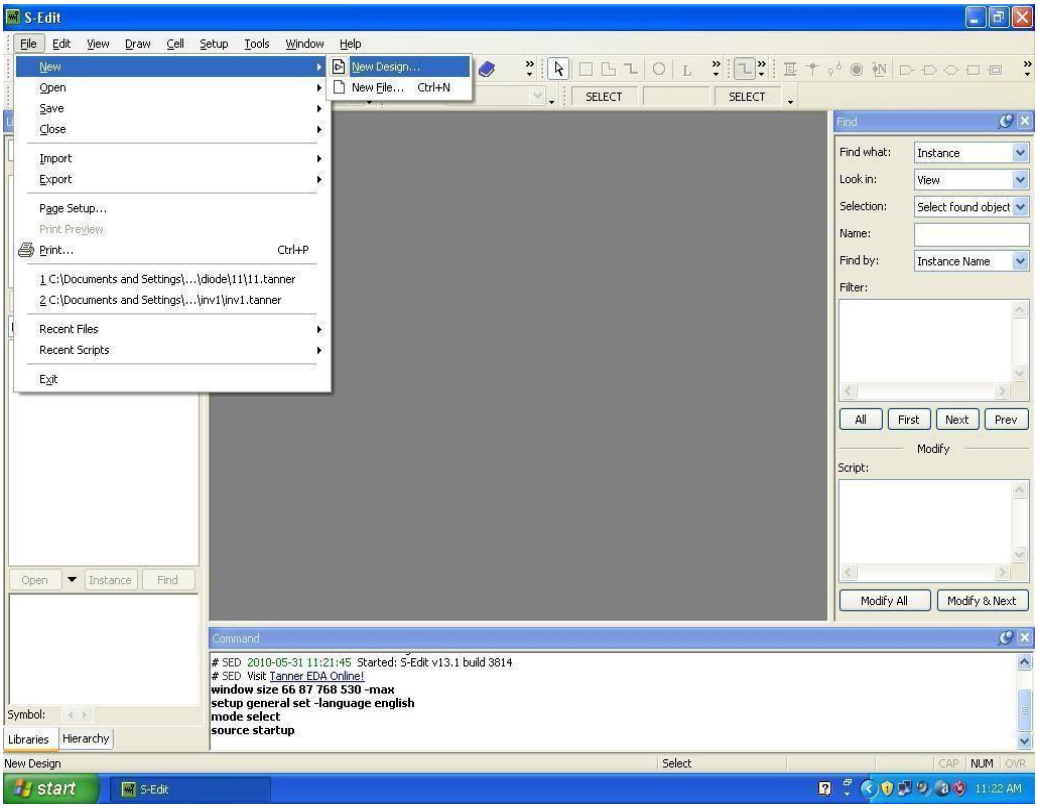
Go to the start menu >>All Programs >>Tanner EDA >>Tanner Tool v 13.0 >> S-Edit v 13.0



A new window will open



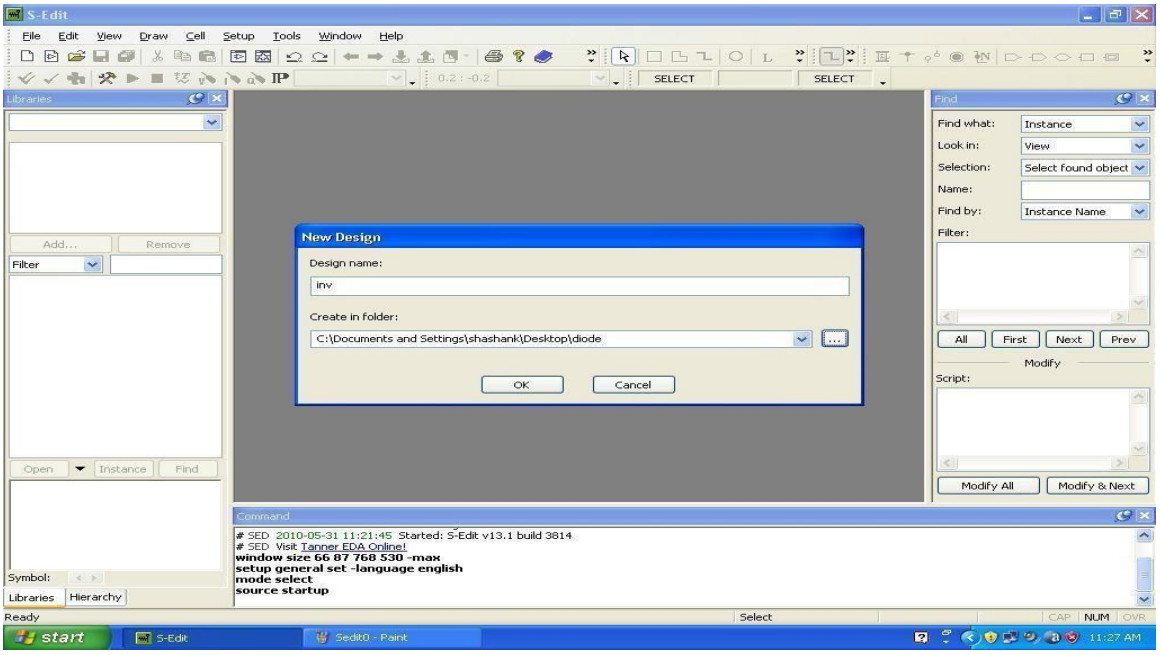
Go to >>file >> New >> New Design Select New Design



One dialog box will appear

Design Name: Give the name your design as you wish

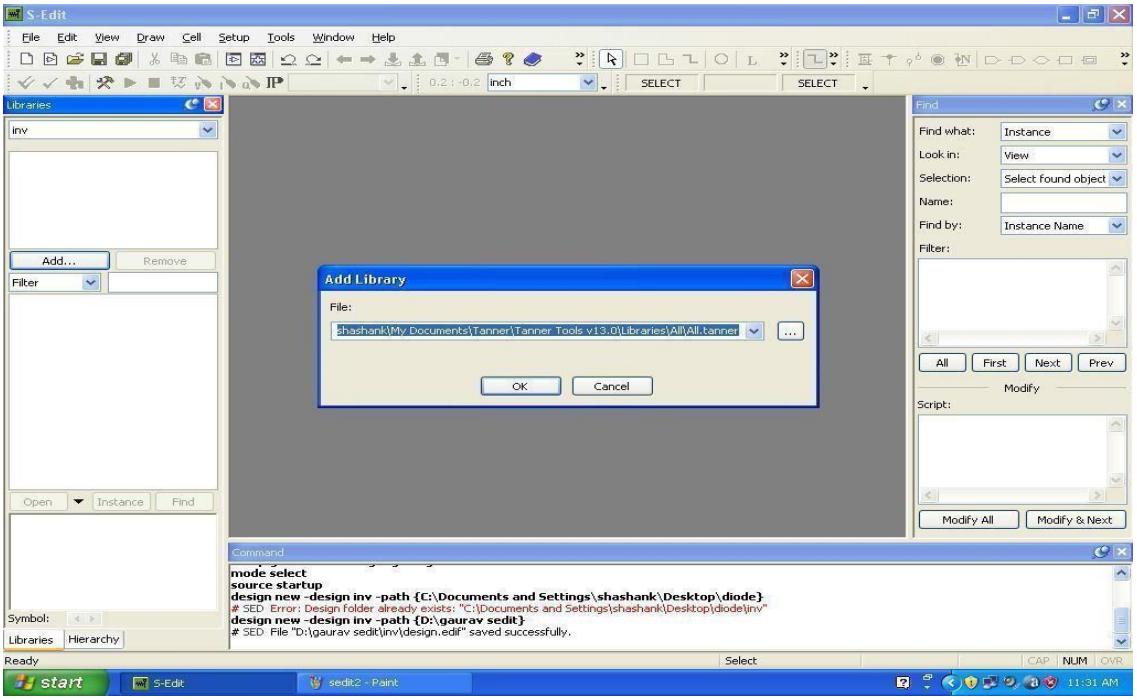
Create a Folder : Give the path where you want to save the S-Edit Files. Then Click on ‘OK’



Now to add libraries in your work click on **Add ,** left on the library window. Give the path

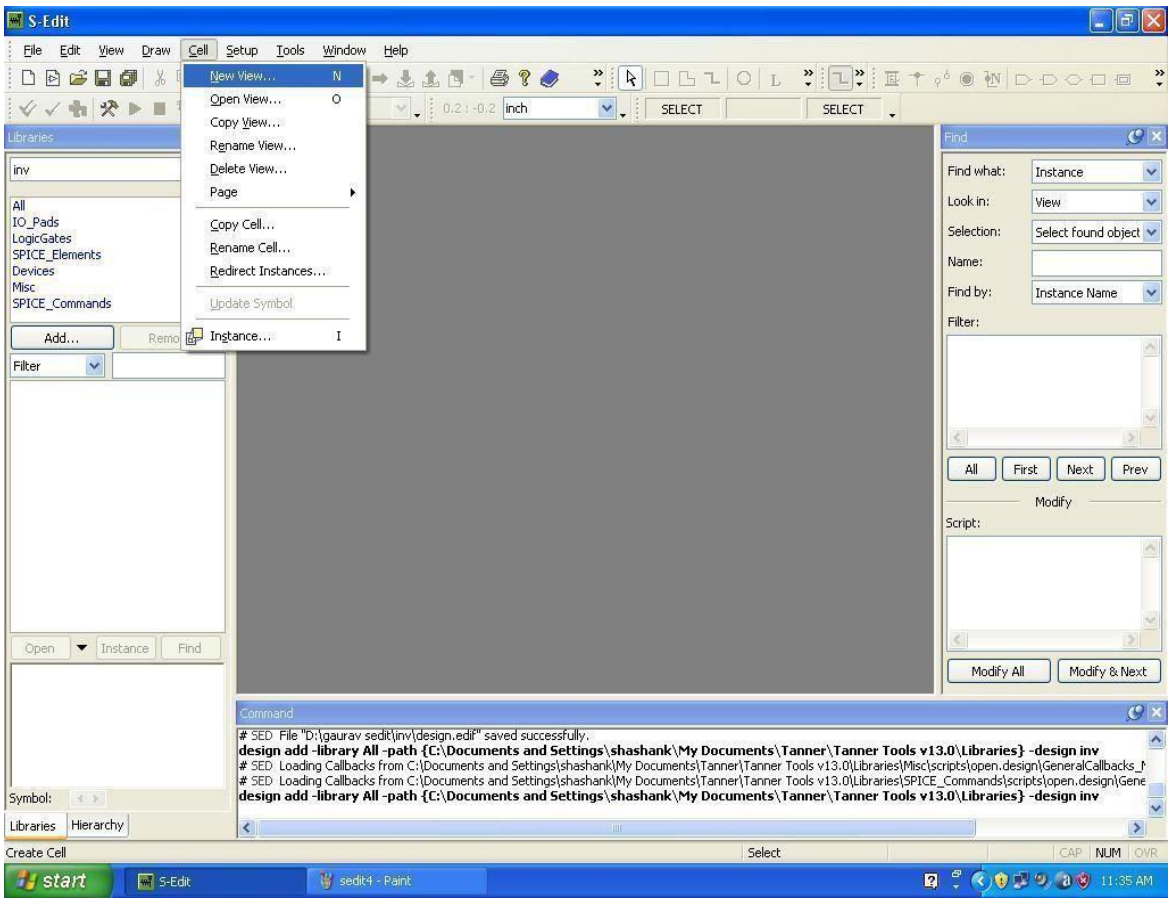
where Libraries are stored . As for example C:\Documents and Settings\Bhowmik.IIIT-3AC288AD0A\My Documents\Tanner EDA\Tanner Tools v13.0\Libraries\All\All. Tanner

By adding the correct library path, you ensure that all necessary design elements, such as transistors, resistors, capacitors, and other predefined circuit components, are available for use in your schematic and layout design. This step is essential for proper circuit simulation and verification, as the software relies on these libraries to interpret and analyze circuit behavior. Properly managing libraries in Tanner EDA helps streamline the **VLSI design process**, improving accuracy and efficiency.



Now to create new cell

Go to cell menu >> New view -- Select ‘New view’



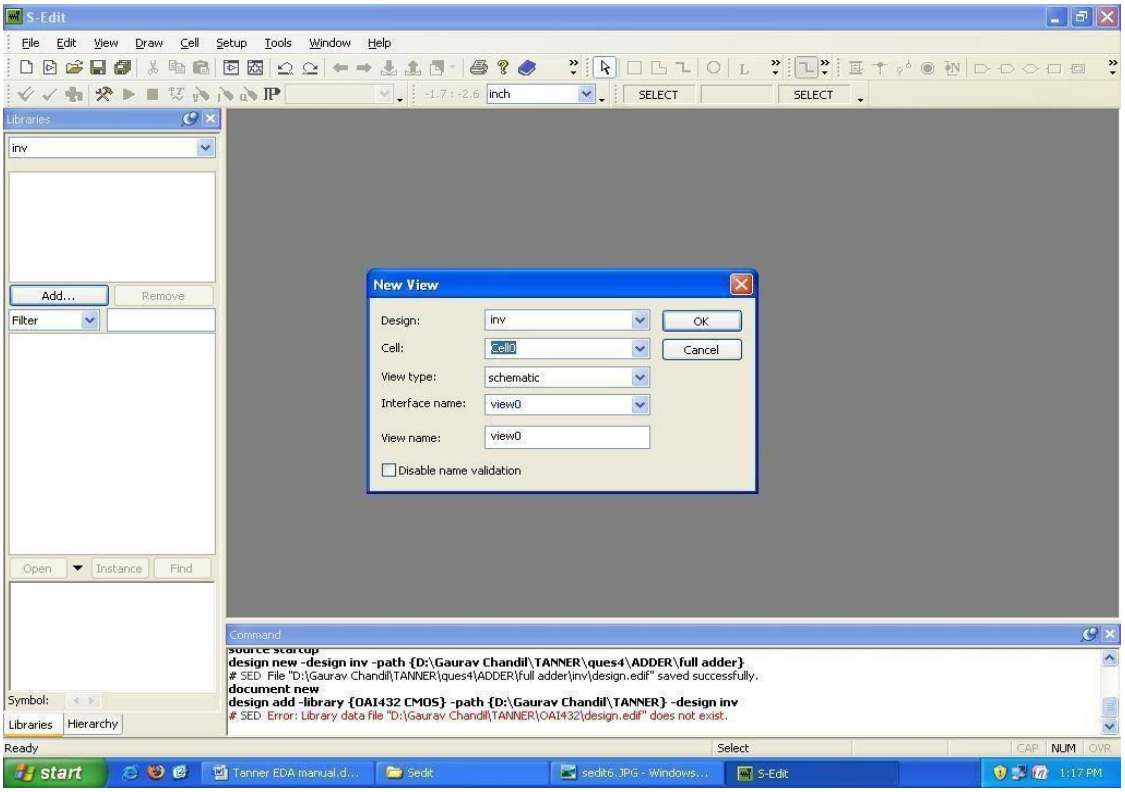
The new cell will appear like below:

Design = your design name

Cell = cell no. (cell no you can change but your design name **inv** will be same for different cell.

Design name should be changed only when you are going to design another circuit) View type = schematic

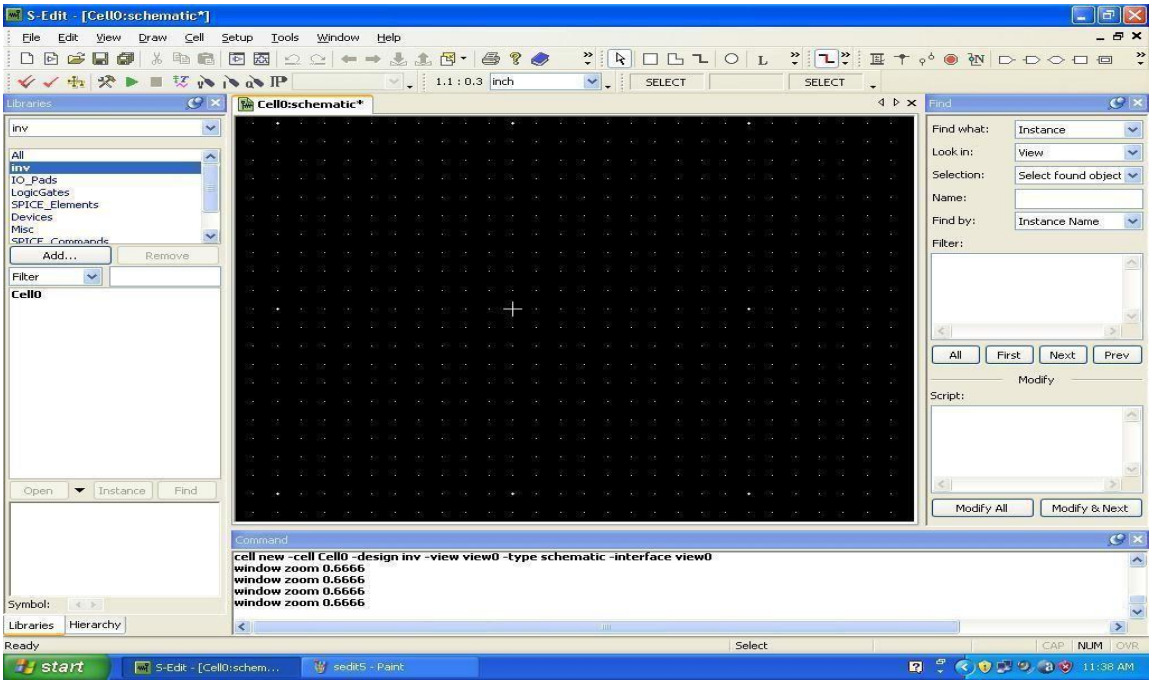
Interface name = “by default” View name = “by default” Then press “OK”.



Then a cell will be appeared where we can draw the schematic of any circuit.

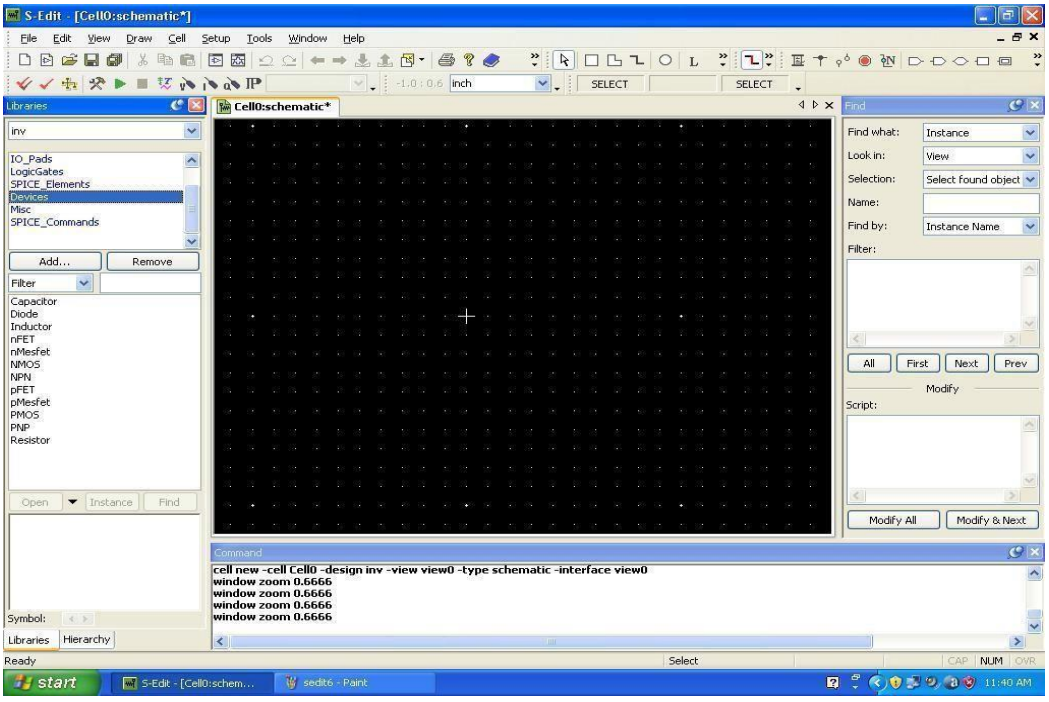
In the black window you have seen some white bubble arranged in specific order. This is called grid. You can change grid distance by clicking on black screen and then scroll the mouse.

If you want your screen big enough for design space, then you can close the **Find** & **command window**. You can again bring these windows from **view** menu bar.



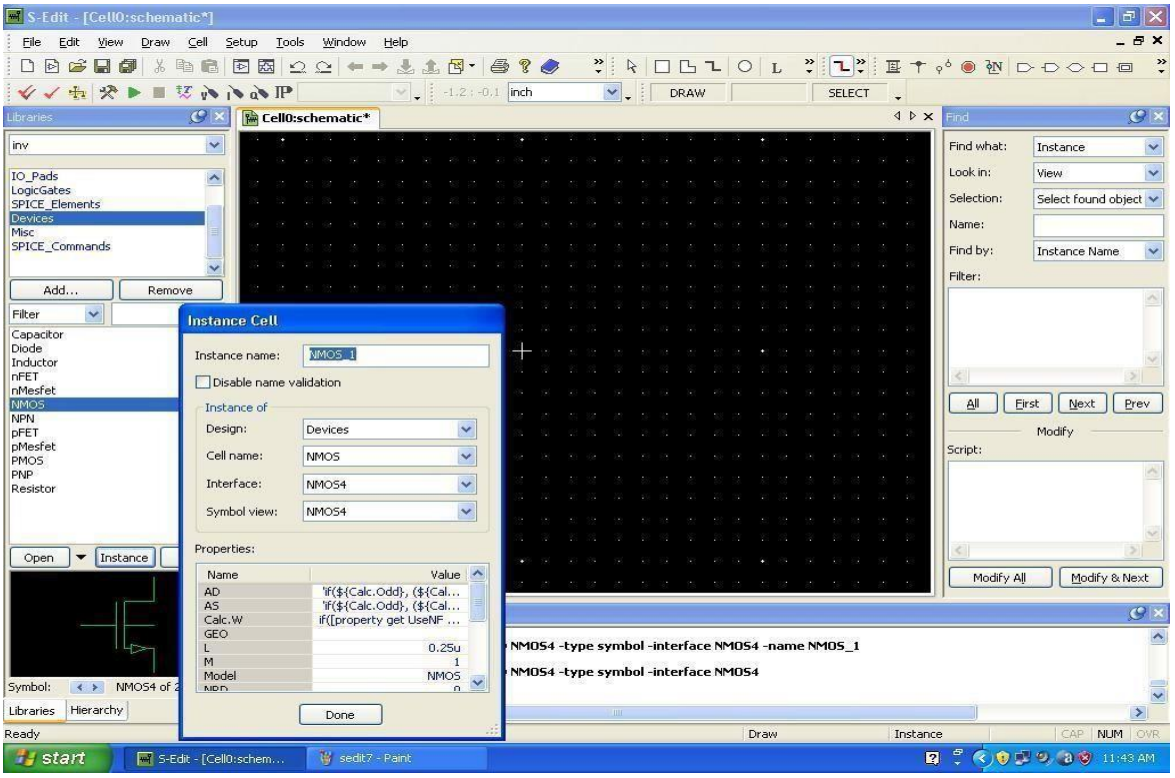
To make any circuit schematic. for example, inverter

a) Go to >>libraries & click on device then all device will be open.



b) Select any device

e.g.: - NMOS Device, then click on, instance (then the dailog box instance cell will appear.)



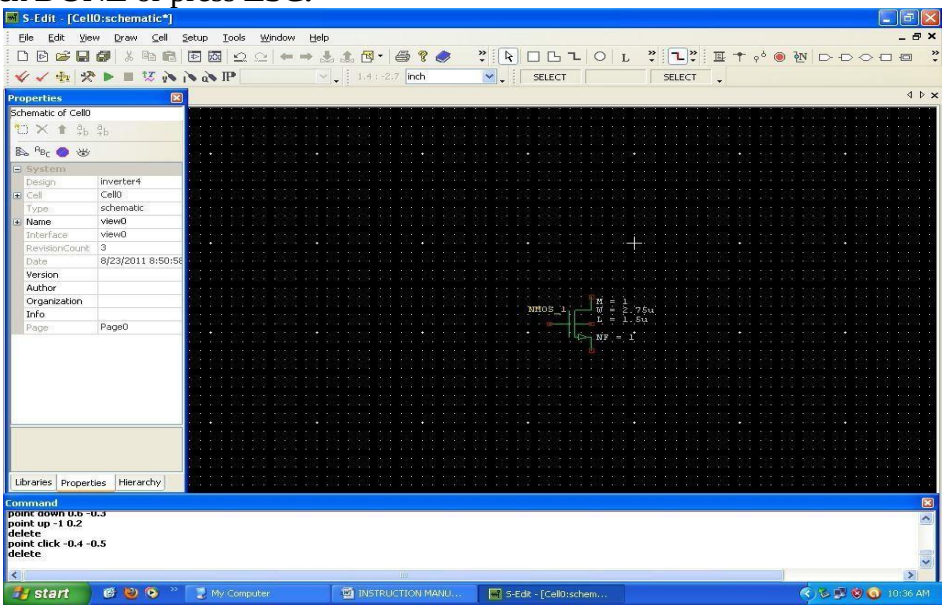
In instance cell

 You can change the values of various device parameters according to your requirements.

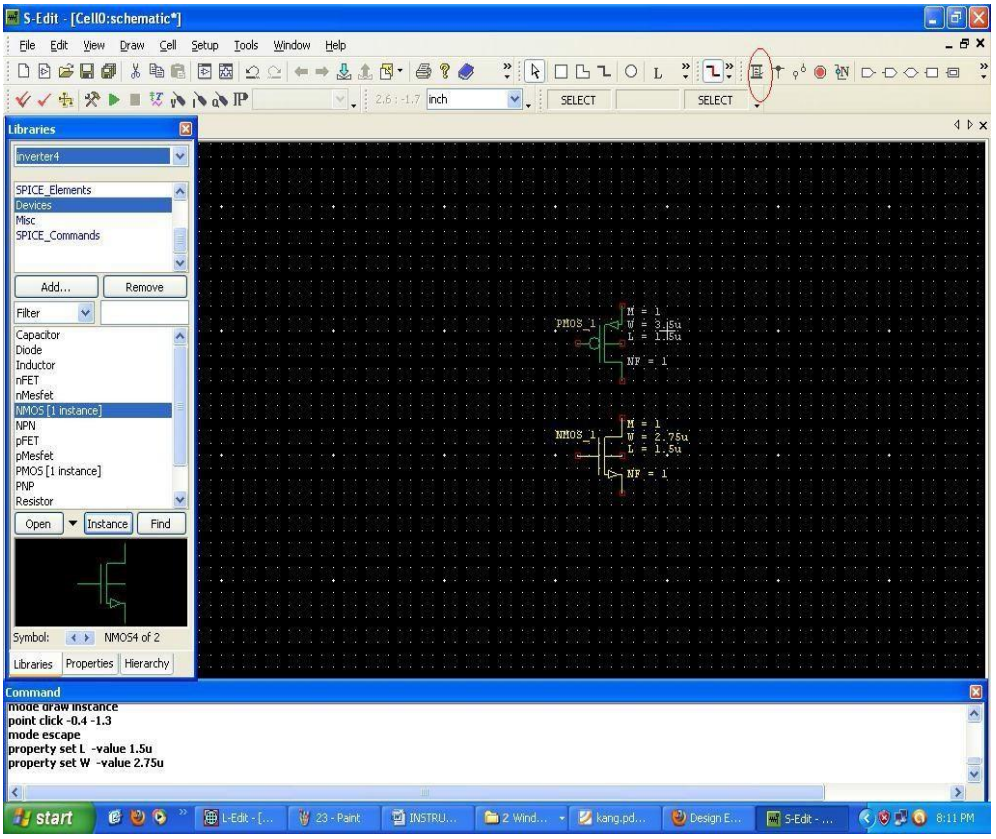
 Go to properties >> change the parameter values as your requirement.

 Now before clicking **DONE,** you have to DRAG the selected device into the cell and drop it where you want it to FIX.

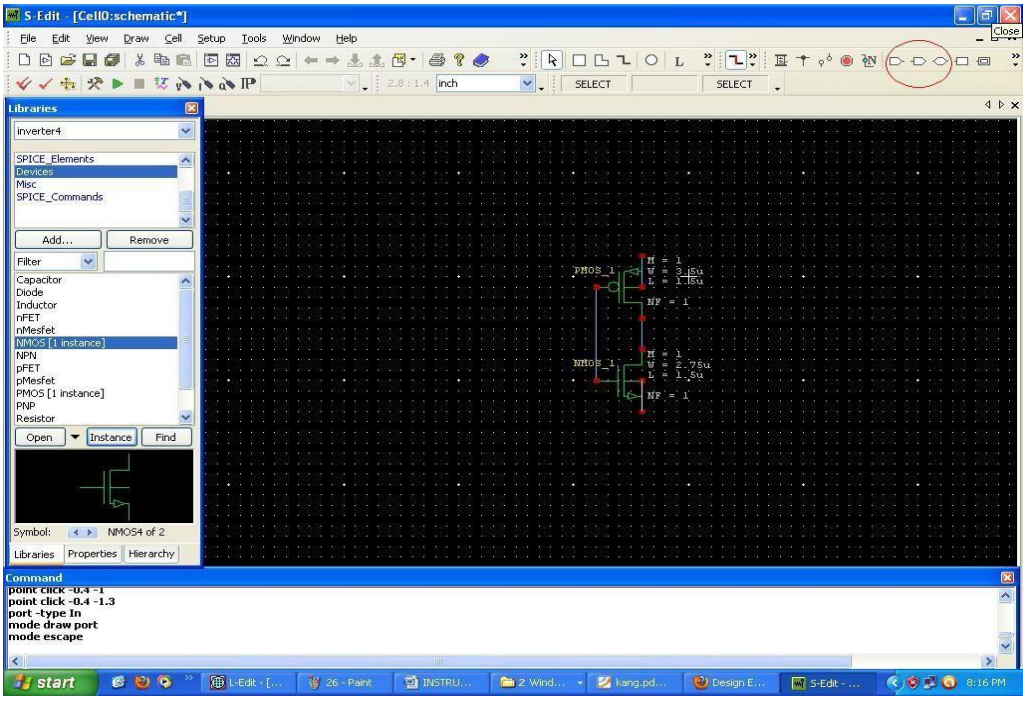
Then click **DONE** or press **ESC.**



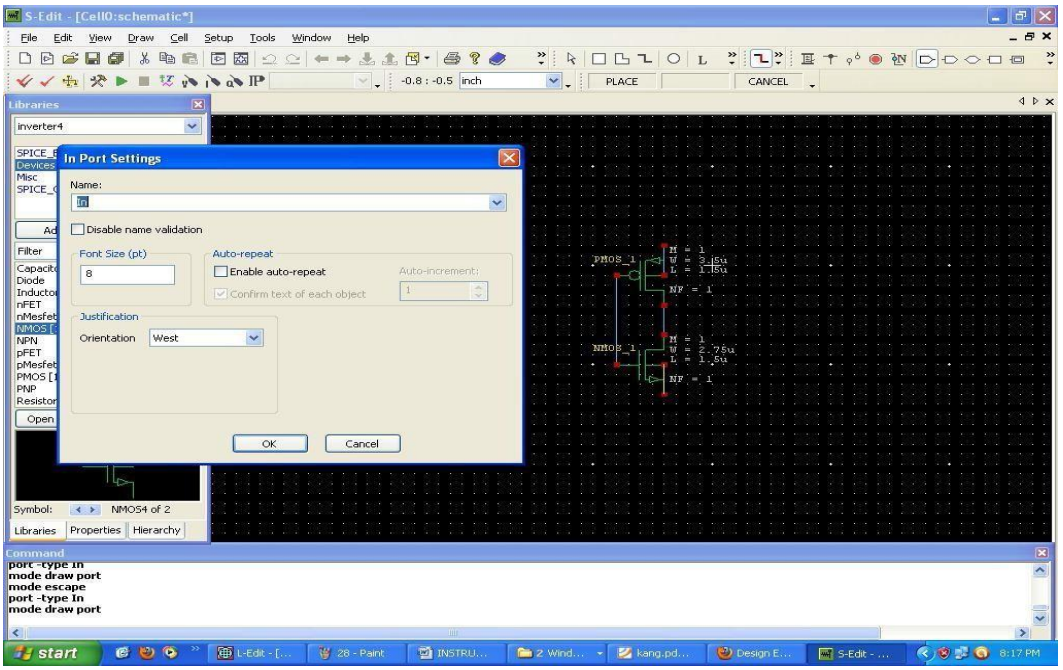
Now connect two devices with wire. Go to tool bar and select wire.



Similarly, to give input & output port in the circuit, select input port that shown by red ellipse.

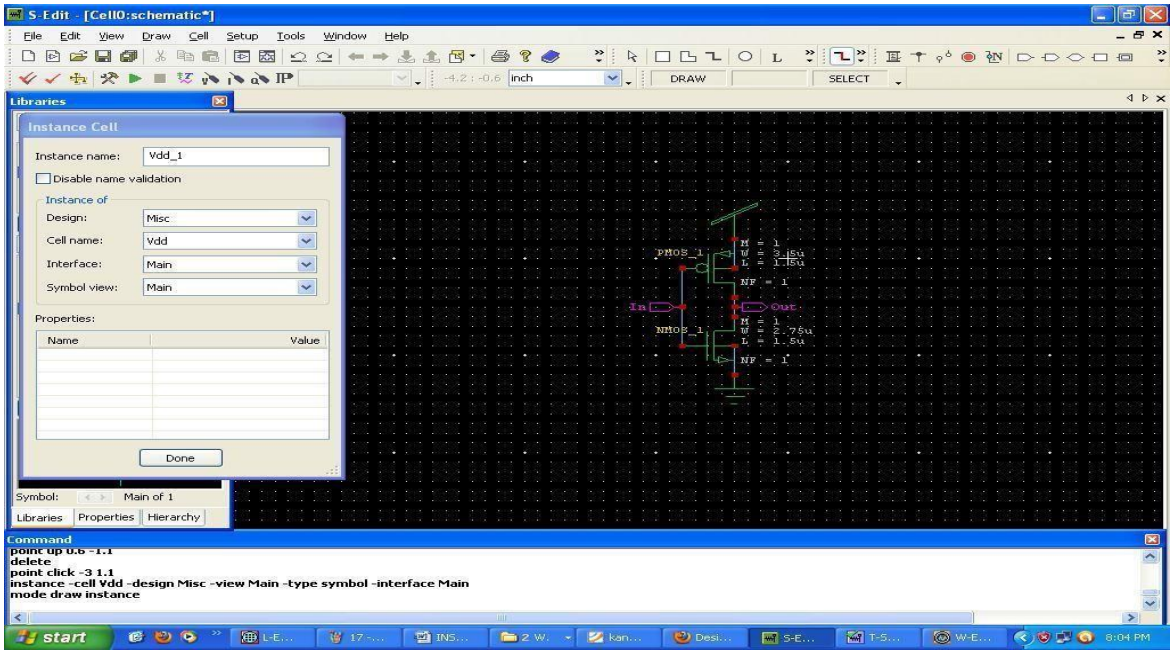


Now you can give Port name as you wish in the dialog box. Then click OK

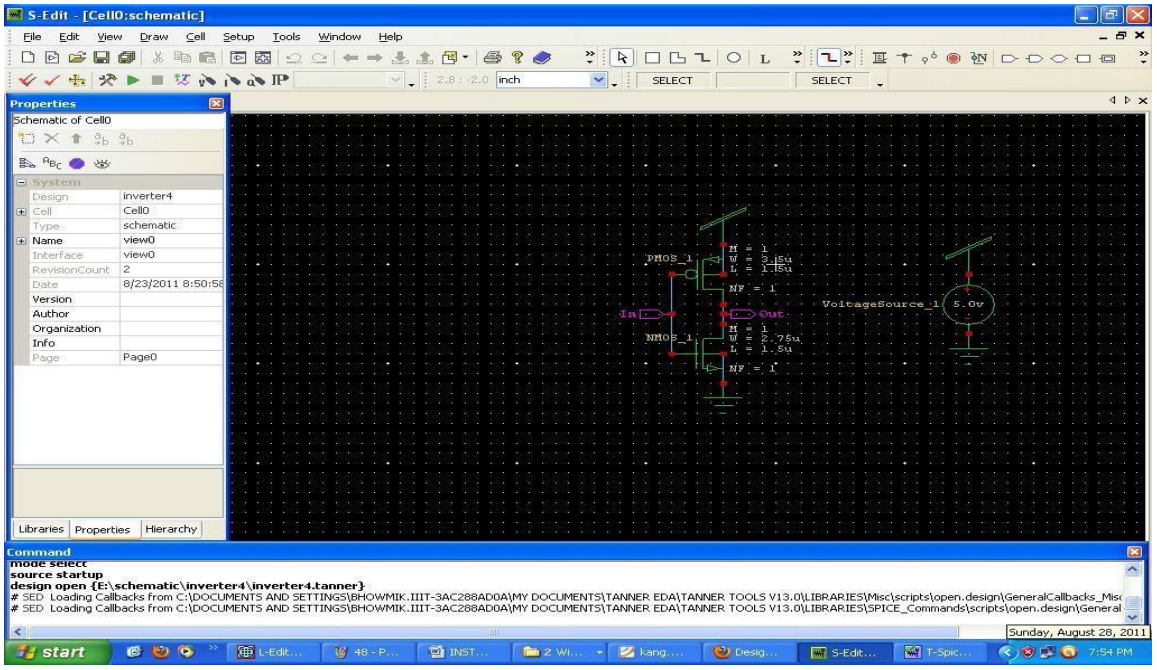


Similarly give Output Port name.

Now, after completed these steps, you should give the supply (VDD) & ground (GND). For that Go to libraries >> MISC >>Select VDD or GND



Now you have to create a source of VDD. For that go to libraries >>spice element >> and then select voltage source of type DC. you can give any value in vdd. let's take vdd =5v.



By doing all the above steps you have completed schematic of Inverter.

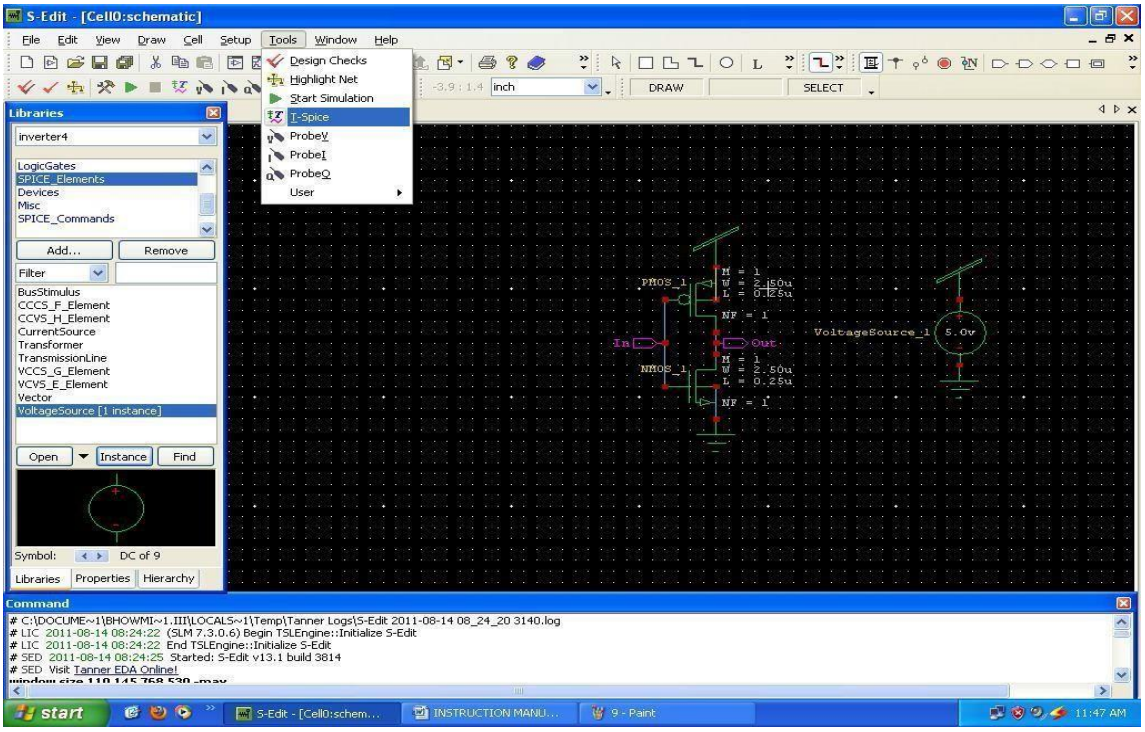
3.3 PRE LAYOUT SIMULATION:

After completing the schematic design, it is essential to verify whether the circuit meets the required specifications. This verification process, known as Pre-Layout Simulation, helps analyze circuit behavior before moving to the physical layout stage. The purpose of this simulation is to ensure functionality, evaluate performance, detect errors, and optimize the design for better efficiency. To begin the simulation in tools like T-Spice, navigate to Tools → T-Spice → OK. Next, define the simulation parameters based on the required analysis, such as DC Analysis for operating points, AC Analysis for frequency response, or Transient Analysis for time-domain behavior. After setting the necessary input conditions, voltage sources, and load parameters, the simulation is executed, and output waveforms are analyzed. If discrepancies arise between expected and actual results, adjustments to component values or configurations are necessary, followed by re-simulation to validate improvements. Once the pre-layout simulation confirms that the circuit meets design specifications, the process moves forward to layout design, where physical placement and routing of components take place while considering parasitic effects and layout-dependent variations.

Once the Pre-Layout Simulation confirms that the circuit meets the design specifications, the next step is Layout Design. In this stage, the physical placement and routing of components are carried out while ensuring that the design adheres to fabrication constraints and design rules. This process involves using Layout Editor (L-Edit) to create a

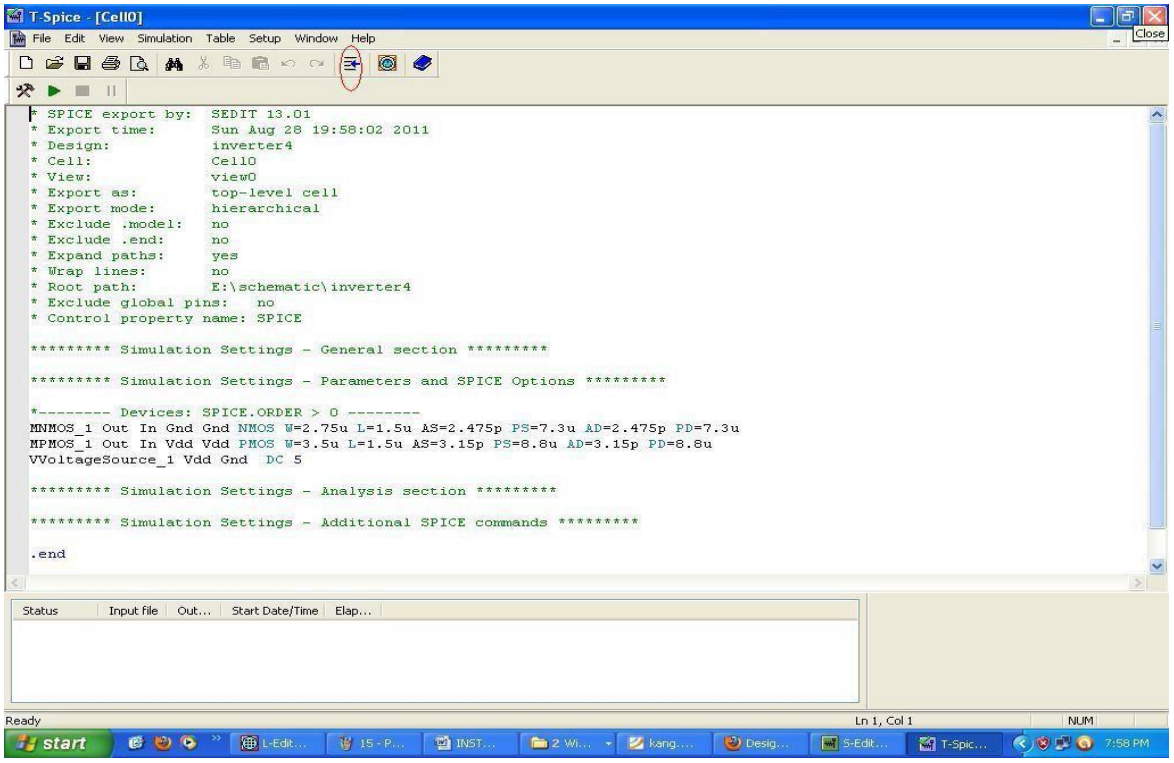
mask layout that represents the final IC structure. The layout must comply with Design Rule Checking (DRC) to avoid manufacturing defects and Layout Versus Schematic (LVS) verification to ensure that the layout matches the original schematic design.

If performance deviations occur in the post-layout analysis, necessary modifications are made to the layout to optimize parameters such as signal integrity, power consumption, and noise margins. Once the circuit passes all verification steps and meets the required specifications, it proceeds to the fabrication stage, where the design is converted into a physical chip. By following a structured approach, including Pre-Layout Simulation, Layout Design, and Post-Layout Simulation.

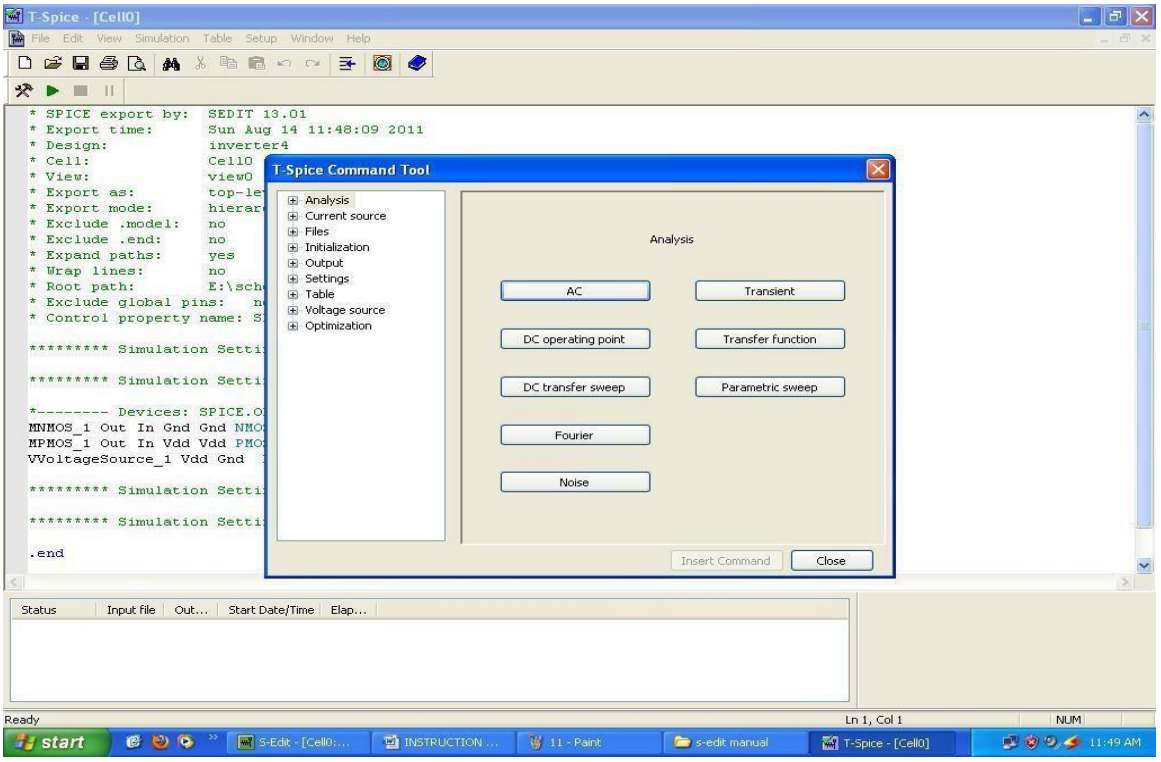


A T-spice window will open.

Then click on the bar shown by red ellipse



A “T-spice command Tool “dialog box will open as shown below.



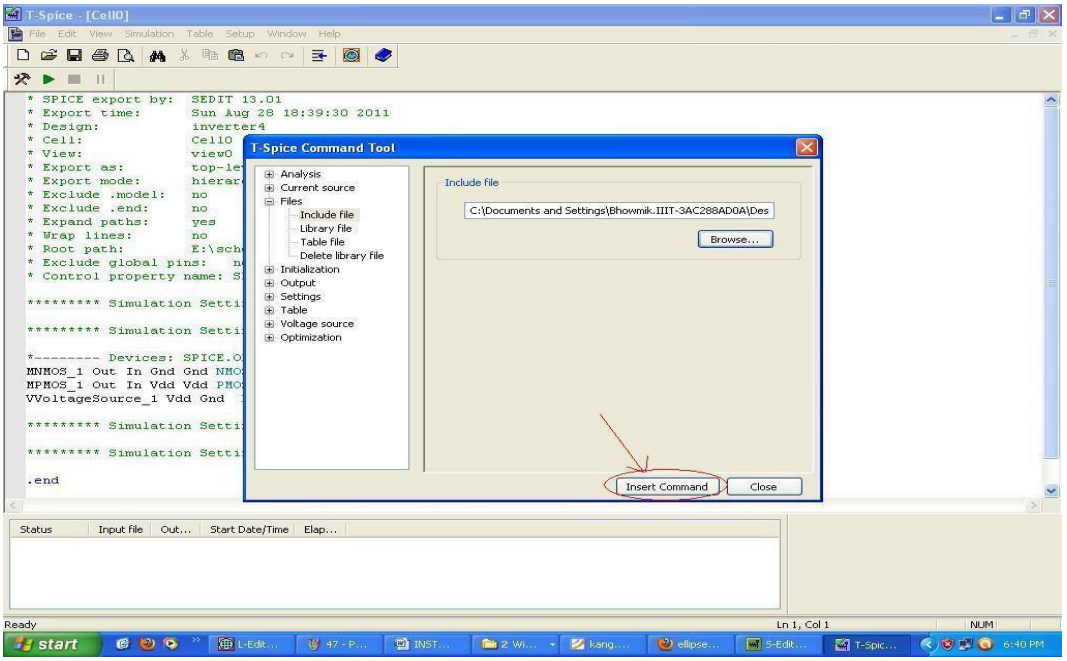
On the T-spice command you can see in the left hand side Analysis,
Current source Files Initialization, Output Settings Table
Voltage source Optimization

Let’s start doing transient analysis of Inverter.

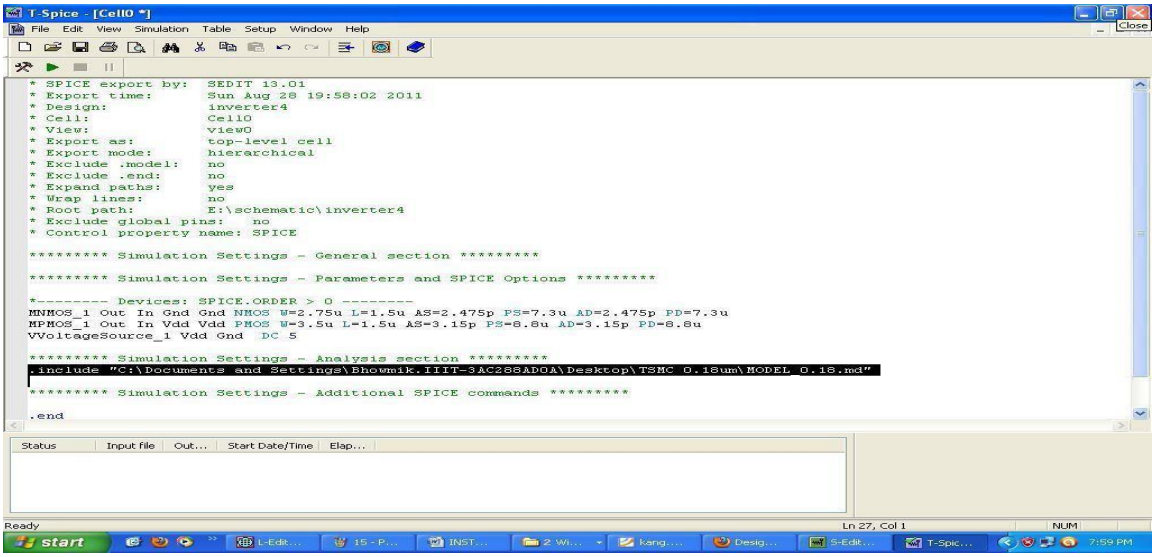
Step 1: You have to include TSMC 0.25 µm Technology file. For that

Go to >> T-spice command tool >> Files >> Include >> browse TSMC .25µm files >> Insert command.

C:\Documents and Settings\Bhowmik.IIIT-3AC288AD0A\Desktop\TSMC 0.25um\MODEL_0.25.md



File is included shown by highlight.



Step2: Then to give Input.

T-spice command tool >> Voltage source >> select type of input you want to give(let’s take **bit**) >> Insert command

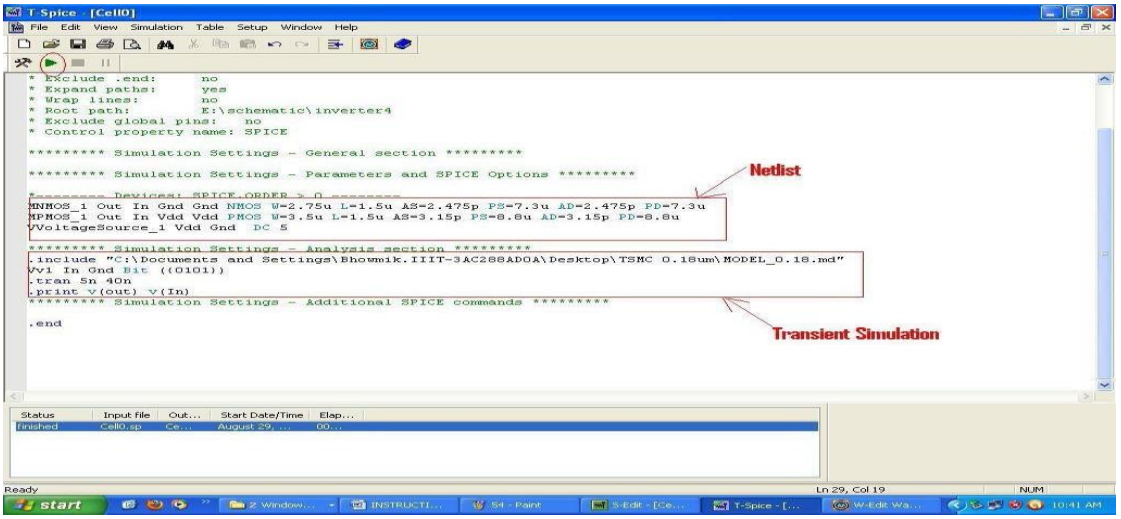
Step 3: Analysis.

T-spice command tool >> Analysis >> select type of analysis you want to give (let's take transient) >> Insert command

step 4: Output.

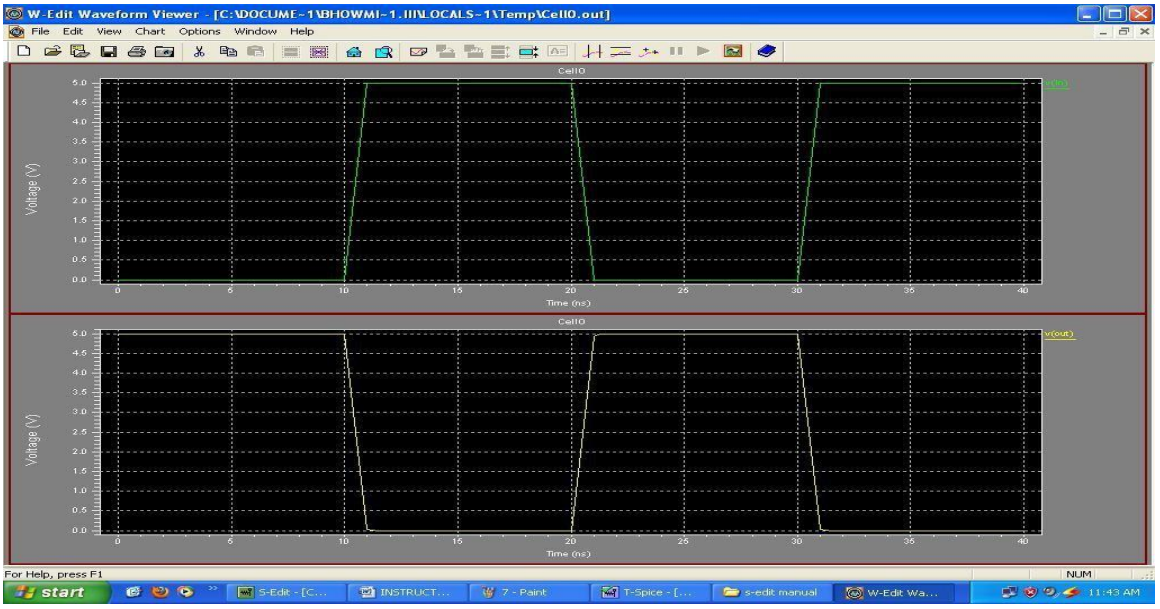
T-spice command tool >> Output >> which output you want to see >> Insert Command

The total spice netlist will come like this.



Now save it.

Then Run by clicking red ellipse shown on left above corner**.** Output of Pre layout simulation of Inverter.



3.4 SIMULATION TOOL

The tool used for simulation purpose for the entire research work is Tanner EDA tool version.13.0. The features and functionality of this tool has been described below: The design cycle for the development of electronic circuits includes an important pre- fabrication verification phase. Because of the expense and time pressures associated with the fabrication step, accurate verification is crucial to efficient design. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit. These simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication. Tanner EDA tool is a complete circuit design and analysis system that includes:

- Schematic Editor (S-Edit): Schematic editor is a powerful design capture and analysis package that can generate netlist directly usable in T-Spice simulations.
- T-Spice Circuit Simulator: T-Spice performs fast and accurate simulation of analog and mixed analog/digital circuits. The simulator includes the latest and best device models available, as well as coupled line models and support for user defined device models via tables or C functions. T-Spice uses an extended version of the SPICE input language that is compatible with all industry standard SPICE simulation programs. All of SPICE's device models are incorporated, as well as resistors, capacitors, inductors, mutual inductors, single and coupled transmission lines, current sources, voltage sources, controlled sources, and a full complement of the latest advanced semiconductor device models from Berkeley and Philips Labs.
- Waveform Editor (W-Edit): W-Edit displays T-Spice simulation output waveforms as they are being generated during simulation. Visualizing the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding, and improving those circuits. W-Edit is a waveform viewer that provides ease of use, power, and speed in a flexible environment designed for graphical data presentation.
- Layout Editor (L-Edit): Tanner EDA tool includes L-Edit for layout editing,• Interactive DRC for real-time design rule checking during editing, Standard DRC for hierarchical DRC, Standard Extract for netlist extraction, Standard LVS for layout versus schematic, Node Highlighting for highlighting all geometry associated with a node and SPR for standard cell place & route.

3.5 T-SPICE

To transform your ideas into designs, you must be able to simulate large circuits quickly and with a high degree of accuracy. That means you need a simulation tool that offers fast run times, integrates with your other design tools, and is compatible with industry standards. Tanner T-Spice Circuit Simulator puts you in control of simulation jobs with an easy-to-use graphical interface and a faster, more intuitive design environment. With key features such as multi-threading support, device state plotting, real-time waveform viewing and analysis, and a command wizard for simpler SPICE syntax creation, T- Spice saves you time and money during the simulation phase of your design flow.

T-Spice enables more accurate simulations by supporting the latest transistor models— including BSIM4 and the Penn State Philips (PSP) model. Given that T-Spice is compatible with a wide range of design solutions and runs on Windows and Linux platforms, it fits easily and cost effectively into your current tool flow.

T-Spice incorporates numerous innovations and improvements not found in other SPICE and SPICE-compatible simulators:

- **Speed**: T-Spice provides highly optimized code for evaluating device models, formulating the systems of linear equations, and solving those systems. In addition to the standard direct model evaluation, T-Spice also provides the option of table-base transistor model evaluation, in which the results of device model evaluations are stored in tables and reused. Because evaluation of device models can be computationally expensive, this technique can yield dramatic simulation speed increases.
- **Convergence:** T-Spice uses advanced mathematical methods to achieve superior numerical stability. Large circuits and feedback circuits, impossible to analyze with other SPICE products, can be simulated in T-Spice.
- **Accuracy**: T-Spice uses very accurate numerical methods and charge conservation to achieve superior simulation accuracy.
- **Macro modeling**: T-Spice simulates circuits containing “black box” macro devices. A macro device can directly use experimental data as its device model. Macro devices can also represent complex devices, such as logic gates, for which only the overall transfer characteristics, are of interest.

- **Input language extensions**: The T-Spice input language is an enriched version of the standard SPICE language. It contains many enhancements, including parameters, algebraic expressions, and a powerful bit and bus input wave specification syntax.
- **External model interface:** You can develop custom device models using C or C++.
- **Runtime waveform viewing**: The W-Edit waveform viewer displays graphical results during simulation. T-Spice analysis results for voltages, currents, charges, and power can be written to single or multiple files.

T-Spice also supports foundry extensions, including HSPICE foundry extensions to models.

- Supports PSP, BSIM3.3, BSIM4.6, BSIM SOI 4.0, EKV 2.6, MOS 9, 11, 20, 30, 31, 40, PSP, RPI a-Si & Poly-Si TFT, VBIC, Modella, and MEXTRAM models.
- Includes two stress effect models, from the Berkeley BSIM4 model and from TSMC processes, in the BSIM3 model to provide more accuracy in smaller geometry processes.
- Supports gate and body resistance networks in RF modeling.
- Performs non-quasi-static (NQS) modeling.
- Supports comprehensive geometry-based parasitic models for multi-finger devices.
- Models partially depleted, fully depleted, and unified FD-PD SOI devices.
- Models self-heating and RF resistor networks.
- Performs table-based modeling for using measured device data to model a device.

Includes enhanced diode and temperature equations to improve compatibility with many foundry model libraries.

Work in a faster, easier design environment:

T-Spice helps integrate your design flow from schematic capture through simulation and waveform viewing. An easy-to-use point-and-click environment gives you complete control over the simulation process for greater efficiency and productivity.

- Enables easy creation of syntax-correct SPICE through a command wizard.
- Highlights SPICE Syntax through a text editor.
- Provides Fast, Accurate, and Precise options to enable optimal balance of accuracy and performance.
- Enables you to link from syntax errors to the SPICE deck by double clicking.
- Supports Verilog-A for analog behavioral modeling, allowing designers to prove system level designs before doing full device level design.
- Provides ". alter" command for easy what-if simulations with netlist changes.

Perform sophisticated analysis:

T-Spice uses superior numerical techniques to achieve convergence for circuits that are often impossible to simulate with other SPICE programs. The types of circuit analysis it performs include:

- DC and AC analysis.
- Transient analysis with Gear or trapezoidal integration.
- Enhanced noise analysis.
- Monte Carlo analysis over unlimited variables and trials with device and lot variations.
- Virtual measurements with functions for timing, error, and statistical analysis including common measurements such as delay, rise time, frequency, period, pulse width, settling time, and slew rate.
- Parameter sweeping using linear, log, discrete value, or external file data sweeps.
- 64-bit engine for increased capacity and higher performance.

With T-Spice, you can

- Optimize designs with variables and multiple constraints by applying a Levenberg-Marquardt non-linear optimizer.
- Perform Safe Operating Area (SOA) checks to create robust designs.
- Use bit and bus logic waveform inputs.

Benefit from flexible licensing

When you purchase a new design tool, licensing options can greatly affect your total cost of ownership. T-Spice is available in node-locked and networked configurations offering you the most flexible licensing possible. With a single solution, T-Spice will work whenever and wherever meeting the design needs of your main workgroup and remote workers. If you offshore design projects, T-Spice does not have geographic restriction on its licenses, thus, lowering your total cost of ownership. Moreover, T-Spice licenses come without geographic restrictions, a major cost-saving factor for organizations involved in offshore or multinational design projects. Unlike tools that impose location-based license limitations, T-Spice enables your global teams to collaborate and access the tool without incurring additional licensing fees or requiring separate regional licenses. This unrestricted access significantly reduces the total cost of ownership (TCO), making T-Spice a practical and scalable solution for growing organizations and complex design environments.

3.6 SCHEMATIC EDITOR

Schematic Editor (S-Edit) is an easy-to-use PC-based design environment for schematic capture. It gives you the power you need to handle your most complex full custom IC design capture. S-Edit is tightly integrated with Tanner EDA's T-Spice simulation, L-Edit layout, and Hipper verification tools. S-Edit helps you meet the demands of today's fast-paced market by optimizing your productivity and speeding your concepts to silicon. Its efficient design capture process integrates easily with third- party tools. S-Edit enables you to explore design choices and provides an easy-to-use view into the consequences of those choices. A faster design cycle gives you more flexibility in moving to an optimal solution—freeing up more time and resources for process corner validation. The results are less risk downstream, higher yield, and quicker time to market.

Schematic capture for the most complex full custom IC design:

- Bus support speeds the creation of mixed signal designs.
- Advanced array support enables easy creation and editing of memory, imaging, or circuits with repetitive blocks.
- Rubber band connectivity editing enables faster design modifications.
- S-Edit displays evaluated parameters in real time over the course of the design process. Parameters with formulas based on other circuit parameters can be displayed or evaluated.
- Auto symbol generation enables you to easily create symbols from schematics, and synchronize any changes.
- All actions are fully scriptable through the TCL/ Tk command language.
- Recordable scripts enable you to automate tasks or expand the tool for application-specific needs.
- Replay-able logs permit recovery if there is an unexpected network or hardware failure.
- S-Edit performs net highlighting and keeps the net highlighted as you move through the hierarchy.
- Cross probe from SPICE net lists and LVS to highlighting nets or devices.
- Schematic ERC enables you to check your design for common errors such as undriven nets, unconnected pins and multiple output pins connected together. The design checks are fully configurable, including custom validation scripts.

Tight integration with simulation:

• S-Edit is tightly integrated with simulation. You can drive the simulator from within the schematic capture environment, viewing operating point results directly on the schematic and performing waveform cross-probing to view node voltages and device terminal currents or charges.

• S-Edit creates an efficient flow for the iterative loop of design, simulation, analysis, and tweaking of circuit parameters. The IC designer can focus on the design and not on data processing—thereby speeding up the design process.

Easy interoperability with third party tools and legacy data

• S-Edit imports schematics via EDIF from third party tools, including Cadence®, Mentor, Laker and View Draw with automatic conversion of schematics and properties for seamless integration of legacy data.

Net lists can be exported in flexible, user-configurable formats, including SPICE and CDL variants, EDIF, structural Verilog, and structural VHDL.

• Library support in S-Edit maximizes the reuse of IP developed in previous projects, or imported from third- party vendors.

Powerful and easy-to-use interface

• S-Edit brings to front-end design capture the ease-of-use and design productivity for which Tanner Tools are known.

• A fully user-programmable design environment allows you to remap hotkeys, create new toolbars, and customize the view to your preference—all in a streamlined GUI.

• The complete user interface is available in multiple languages. S-Edit currently supports English, Japanese, Simplified and Traditional Chinese.

• S-Edit provides Unicode support. All user data can be entered in international character sets.

Cost-effective

• S-Edit provides an ideal performance to-cost ratio, allowing you to maximize the number of designers on a project.

• Since S-Edit is Windows-based, designers can work on cost-effective workstations or laptops. This means you can take your work with you anywhere—even home—and continue working to meet time-to-market pressures.

• Available in two configurations—full schematic editor, and schematic viewer.

Easy to manage

• Human-readable technology files and design databases are revision-control system-compatible.

• CAD managers can control distribution and access rights to the technology or design. The format allows revision control systems to manage revisions over the course of the design process.

Benefit from flexible licensing

When you purchase a new design tool, licensing options can greatly affect your total cost of ownership. S-Edit is available in node-locked and networked configurations offering you the most flexible licensing possible. With a single solution, S-Edit will work whenever and wherever meeting the design needs of your main workgroup and remote workers. If you offshore design projects, S-Edit does not have geographic restriction on its licenses, thus, lowering your total cost of ownership.

One of the significant advantages of S-Edit is its lack of geographic restrictions, meaning that offshore design projects and remote teams can seamlessly use the software without additional licensing constraints. This ensures uninterrupted workflow, better resource utilization, and a lower total cost of ownership, particularly for companies operating across multiple locations. Additionally, with a single licensing solution, S- Edit ensures that your primary design team and remote engineers can work efficiently without limitations, improving overall productivity and project scalability. The flexibility in licensing makes S-Edit a cost-effective and accessible solution for modern design environments, whether for small businesses, startups, or large enterprises managing global design teams.

On the other hand, networked licenses allow multiple users within a network to access the tool, making it a more efficient choice for collaborative and distributed teams.

3.7 MEMORY

Memory is a storage part in a computer system. It is used to store the data, information, and programs at the time of processing on the computer. It stores data either temporarily or permanent. The main use of memory is saving and retrieving data.

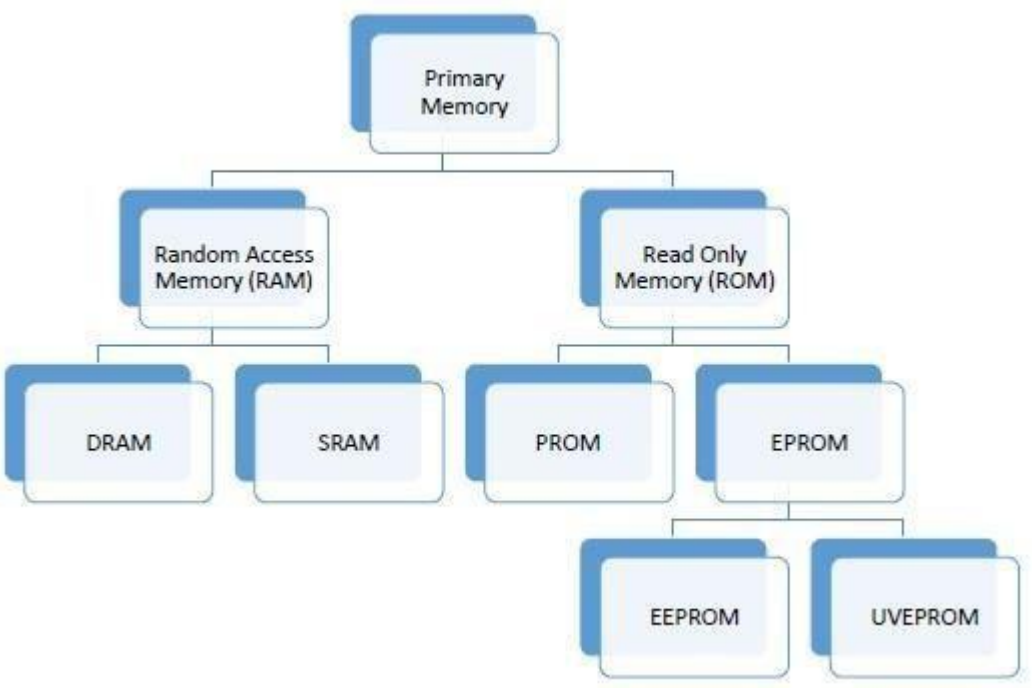


Fig 3.1: Types of Memory

Types of Memory

Generally, computer system consists of two types of memory −

Primary Memory or Volatile Memory

It is called the internal memory of the computer. And it is also known as main memory or Temporary memory. It holds the data and instructions that are presently working on the system or by the CPU. Primary Memory is called volatile memory, because when power is switched off it loses all data.

Primary memory is generally of two types:

- RAM
- ROM

RAM (Random Access Memory) - It stands for Random Access Memory. RAM is a read /writes memory. It is referred as main memory of the computer system. It is a temporary memory. The information stored in RAM is lost whenever the power supply to the computer is switched off.

RAM is also of two types which are as follows –

- **Static RAM** − Static RAM also known as SRAM. In this RAM the information is stored as long as the power supply is ON. SRAM are of higher coast and consume more power. They have higher speed than Dynamic RAM.
- **Dynamic RAM** − Dynamic RAM also known as DRAM, This type of RAM stores information in a very short time basically, a few milliseconds even though the power supply is ON. The Dynamic RAM is cheaper and of moderate speed and also they consume less power.

ROM (Read Only Memory) − It stands for Read Only Memory. ROM is a permanent type of memory. ROM information is not lost when power supply is switched off. The Content of ROM is inserted by the computer manufacturer and permanently stored at the time of manufacturing. ROM cannot be overwritten by the computer. It is also called Non-Volatile Memory.

ROM memory has three types' names which are as following –

- **PROM (Programmable Read Only Memory)** − It is used to write data once and read many. Once a chip has been programmed, the recorded information cannot be changed. It is a non- volatile memory.
- **EPROM (Erasable Programmable Read Only Memory)** − EPROM chip can be programmed by erasing the information stored earlier in it. Information stored in EPROM exposing the chip for ultraviolet light.
- **EEPROM (Electrically Erasable Programmable Read Only Memory)** − It is programmed and erased by special electrical waves in milliseconds. A single byte of data or the entire contents of the device can be erased.

3.8 RANDOM ACCESS MEMORY (RAM):

Random access memory (RAM) is a type of primary storage. It allows the user to randomly access any part of the data regardless of its position in roughly the same time. This is not possible using other storage devices such as hard disks, CD's etc. because they have physical constraints such rotation speeds, arm movements etc.

RAM is mostly volatile i.e. the data in RAM is dependent on the power and as lost when power is switched off. However, there are some non - volatile versions of RAM also available.

There are mainly two types of RAMS available i.e. Static RAM (SRAM) and Dynamic RAM (DRAM). SRAM is very fast and power-efficient because it uses flip-flop circuits to store data, but it is also expensive and takes up more space, making it ideal for cache memory inside processors. On the other hand, DRAM stores data using small capacitors that need frequent refreshing, making it cheaper and capable of storing more data than SRAM, though it is slightly slower and consumes more power. DRAM is commonly used in computer memory (RAM modules), smartphones, and servers. The more RAM a system has, the smoother it runs, especially for demanding tasks like gaming, video editing, and multitasking.

Details about these are given as follows:

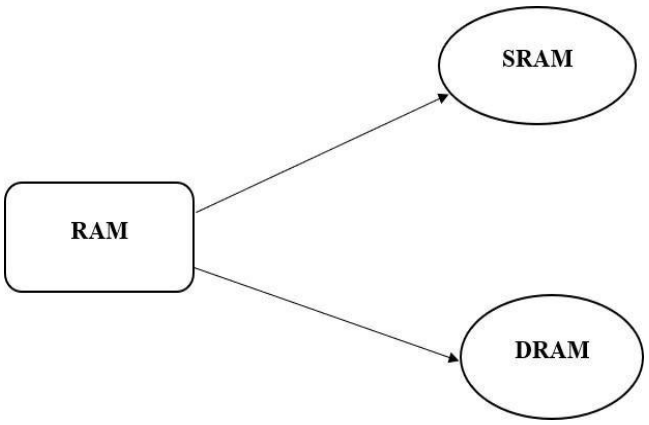


Fig 3.2: Types of RAM

Static Random Access Memory (SRAM):

SRAM is a type of semiconductor memory that uses flip flops to store the bits. SRAM is volatile even though it exhibits data remanence i.e. residual data even after repeated deletion

attempts.

SRAM is more expensive than DRAM and consequently is used to create the cache while DRAM is used to create the main memory. The word static indicates that the memory retains its contents as long as power is being supplied. However, data is lost when the power gets down due to volatile nature. SRAM chips use a matrix of 6-transistors and no capacitors. Transistors do not require power to prevent leakage, so SRAM need not be refreshed on a regular basis.

There is extra space in the matrix, hence SRAM uses more chips than DRAM for the same amount of storage space, making the manufacturing costs higher. SRAM is thus used as cache memory and has very fast access.

SRAM Basics

There are two key features to SRAM - Static Random Access Memory, and these set it out against other types of memory that are available:

- **The data is held statically:** This means that the data is held in the semiconductor memory without the need to be refreshed as long as the power is applied to the memory.
- **SRAM memory is a form of random-access memory:** A random-access memory is one in which the locations in the semiconductor memory can be written to or read from in any order, regardless of the last memory location that was accessed.

The circuit for an individual SRAM memory cell comprises typically four transistors configured as two cross coupled inverters. In this format the circuit has two stable states, and these equate to the logical "0" and "1" states.

The transistors are MOSFETs because the amount of power consumed by MOS circuit is considerably less than that of bipolar transistor technology which is the other feasible option, but it will consume much more

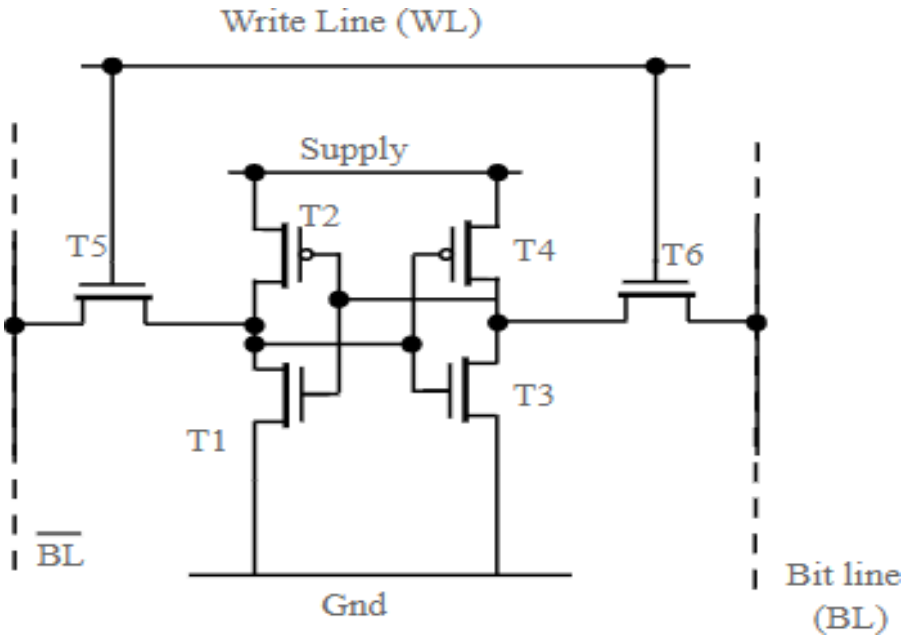


Fig 3.3: 6T SRAM

Sometimes further transistors are used to give either 8T memory cells. These additional transistors are used for functions such as implementing additional ports in a register file, etc. for the SRAM memory. Although any three terminal switch devices can be used in an SRAM, MOSFETs and in particular CMOS technology is normally used to ensure that very low levels of power consumption are achieved. With semiconductor memories extending to very large dimensions, each cell must achieve a very low levels of power consumption to ensure that the overall chip does not dissipate too much power.

SRAM memory cell operation:

The operation of the SRAM memory cell is relatively straightforward. When the cell is selected, the value to be written is stored in the cross-coupled flip-flops.

The cells are arranged in a matrix, with each cell individually addressable.

Most SRAM memories select an entire row of cells at a time, and read out the contents of all the cells in the row along the column lines. While it is not necessary to have two-bit lines, using the signal and its inverse, this is normal practice which improves the noise margins and improves the data integrity. If the two lines are the same, then the system will understand there is an issue and re-interrogate the cell.

The two-bit lines are passed to two input ports on a comparator to enable the advantages of the differential data mode to be accessed, and the small voltage swings that are present can be more accurately detected. Access to the SRAM memory cell is enabled by the Word Line. This controls the two access control transistors which control whether the cell should be connected to the bit lines. These two lines are used to transfer data for both read and write operations.

Characteristic of Static RAM

- Long life
- No need to refresh
- Faster
- Used as cache memory
- Large size
- Expensive
- High power consumption

SRAM memory applications:

There are many different types of computer memory that are available these days. Choices need to be made regarding the correct memory type for a given application.

Possibly two of the most widely used types are DRAM and SRAM memory, both of which are used as microcontroller / microprocessor and computer memory. Of these two SRAM is more expensive than DRAM. However, SRAM is faster and consumes less power especially when idle.

In addition to this SRAM memory is easier to control than DRAM as the refresh cycles do not need to be taken into account, and in addition to this the way SRAM can be accessed is more exactly random access. A further advantage if SRAM is that it is denser than DRAM.

As a result of these parameters, SRAM memory is used where speed or low power are considerations. Its higher density and less complicated structure also lend it to use in semiconductor memory scenarios where high-capacity memory is used, as in the case of the working memory within computers.

Microcontrollers which incorporate battery-backed, non-volatile SRAM are widely used in the embedded computing arena. Unlike Flash memory or EEPROM technology,

non-volatile SRAM has no write limitations, i.e. no limitations on the number of write / read cycles which makes it ideal for real-time data logging applications.

Although SRAM does not have the capabilities of some forms of computer memory, it is nevertheless widely used for applications like handling caches in computers and especially in microcontrollers where is speed, low power and simpler operation lend it to these situations far more than DRAM, Flash and other forms of computer memory.

Advantages of SRAM

- It is relatively simple to handle a SRAM.
- SRAM results in a lower power consumption that DRAM.
- SRAM is quite reliable and so it is used as cache memory in computer systems

Dynamic RAM (DRAM):

DRAM, unlike SRAM, must be continually refreshed in order to maintain the data. This is done by placing the memory on a refresh circuit that rewrites the data several hundred times per second. DRAM is used for most system memory as it is cheap and small. All DRAMs are made up of memory cells, which are composed of one capacitor and one transistor.

DRAM is a type of semiconductor memory that uses capacitors to store the bits. The charging and discharging of the capacitor represents 0 and 1 i.e. the two possible values that can be stored in a bit. The DRAM is a volatile memory i.e. the data in memory is lost when power is switched off. However, it still displays some data remanence. DRAM is low cost compared to SRAM so it is primarily used in main memory.

Characteristics of Dynamic RAM:

- Short data lifetime
- Needs to be refreshed continuously
- Slower as compared to SRAM
- Used as RAM
- Smaller in size
- Less expensive
- Less power consumption

Uses of RAM

RAM is usually used as main memory i.e. temporary storage for computer applications and operations. However, it has many other uses as well. Some of these are given as follows:

Virtual memory

Operating systems use a part of RAM to implement paging. This leads to an illusion that memory is more than it actually is. This is known as virtual memory. However, paging should only be used to a limit or it results in thrashing.

RAM disk

A RAM disk is a section of the computer's RAM that is used as if it were a hard drive. Since RAM is much faster than traditional storage devices like HDDs or SSDs, a RAM disk can significantly improve data access speeds. However, because RAM is volatile, all data stored in a RAM disk is lost when the computer is turned off, unless there is a backup power source or a mechanism to save the data before shutdown. RAM disks are often used for temporary file storage, caching, and improving the performance of certain applications that require frequent read/write operations.

Shadow RAM

Shadow RAM is created when the contents of a slow ROM (Read-Only Memory) are copied into faster read/write memory (RAM). The system then switches the memory locations, allowing the processor to access the ROM content at higher speeds. This process, known as shadowing, improves system performance by reducing delays caused by slow ROM access. Shadow RAM is commonly used in BIOS firmware and embedded systems where frequent access to ROM-stored data is required. Since RAM is much faster than ROM, shadowing helps optimize the system’s overall efficiency.

3.9 7T SRAM

As like 6T SRAM, the 7T SRAM circuit also consists of two CMOS cross coupled to each other. In this circuit we additionally connect NMOS transistor to write line. And it also has two pass NMOS transistor connected to the bit and bit bar line. The access transistor N3 and N4 which are correspondingly connected to the write and read line to perform the write and read operation. Before write operation the 7T SRAM cell depends upon feedback connection. These feedback connection and disconnection can be performed by N5 transistor.

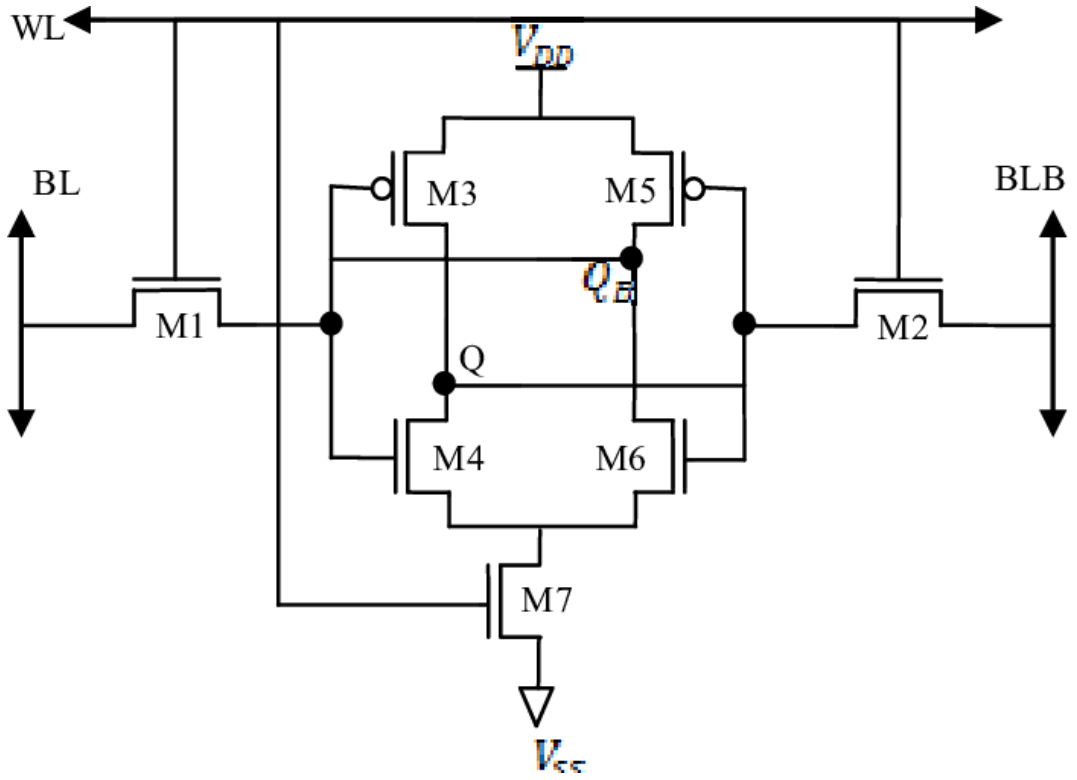


Fig 3.4: 7T SRAM

Write Operation

The write operation can be start by turning off the N5 transistor to this cut off feedback connection. When N3 is on and N4 is off the bit line bar carries complement of input data. The N5 is turned on and WL is turned off for reconnect the feedback connection to store new data. The bit line bar is discharged to "0" for storing "1" in the cell. And there is no need to discharge bit line for storing "0" in the cell.

Read Operation

When performing the read operation both read and word lines are turned to on and also the transistor N 5 is kept on.

3.10 8T SRAM

In this paper a single ended 8T SRAM cell with high read stability is proposed. Figure represents the proposed cell. It utilizes a single bit line and two separate word lines WWL and RWL for write and read operation respectively. The proposed cell has two cross coupled inverters, left inverter has three transistors P-2, N-1, N-3 and right inverter has two transistors P-1, and N-2. The proposed cell uses an extra transistor CS to cut off the feedback in cross coupled inverters. In proposed cell the read and write operation are controlled by

separate word lines, which enhances the write ability and read stability of the cell. The write word-line WWL is used to transfer data from single bit-line BL to Q and the inverted information is stored at QBAR. When read word line RWL is activated, the bit line BL is used to transfer data from the cell as the output during read operation. In this proposed cell the stored data at node Q, passes through the PMOS_3 transistor, which control the read operation of the cell. When 0 is stored at node Q, PMOS_3 turn ON and while enabling RWL the charged stored at bit line discharges through the transistors PMOS_3 and NMOS_5.

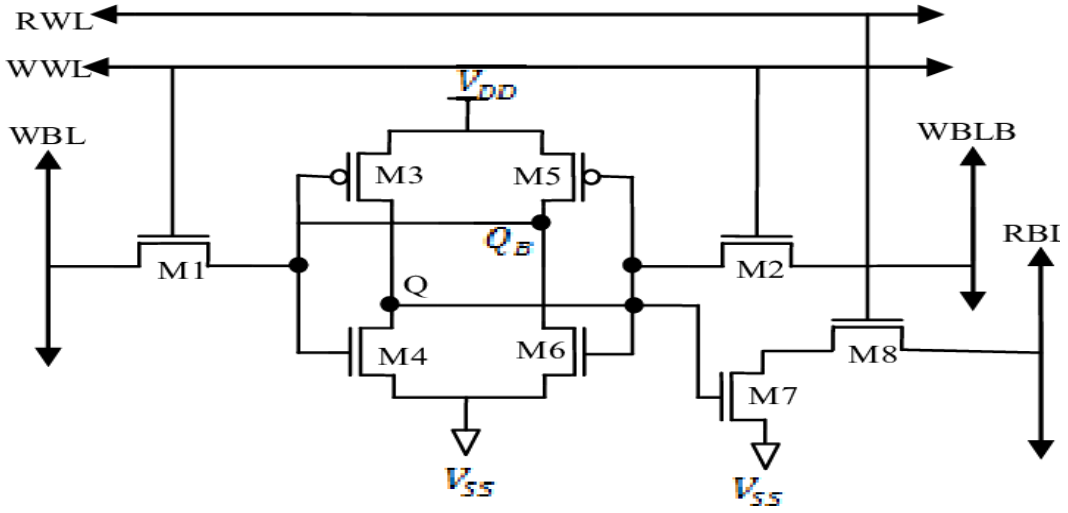


Fig 3.5: 8T SRAM

Sense amplifier detects the stored 0 at Q. when 1 is stored at node Q, the connected PMOS_3 transistor remains off. That forces the BL to charged at 1 and sense amplifier read the stored 1.

Write Operation

Prior to write 1 at node Q, bit line is charged to VDD and write word line is pulled high. During write operation CS is maintained at 0v, to retain the stored content at node Q. During write '0' the bit line is maintained at ground and signal CS at VDD, so that the charge stored at node Q can easily be inverted from 1 to 0. Which speed up the write operation and write ability of the proposed 8T SRAM cell.

Read Operations

Before initiating the read operation, BL is kept at VDD while WWL and RWL are maintained at 0v and VDD respectively. In the proposed cell the storing node Q is directly connected to the PMOS (P_3) transistor. During read 1 operation P_3 gets turn off due to

stored 1 at Q, RWL is activated. The pre-charged BL not get discharged due to turn off state of P_3, and 1 is read by sense amplifier. If ‘0’ is stored at node Q, the connected PMOS gets turn on and when RWL is activated, the whole charged stored at BL is discharged through P_3 and N_5 and ‘0’is sensed by the sense amplifier.

3.11 9T SRAM

9T SRAM proposed in then carry out performance evaluation with the conventional 6T SRAM topologies in terms of stability, process variation and current leakage so as to justify the performance evaluation.

Read Operation:

This configuration employs a differential read operation for better read access time and the design should be made symmetrical. During read operation, RWL is activated and transistors MN5 and MN6 are turned ON which will form strong pull down compared with conventional 6T SRAM. Thus, strong pull-down results to less resistance between data storage nodes to ground; therefore, the amount of raise in voltage of node Q will be less.

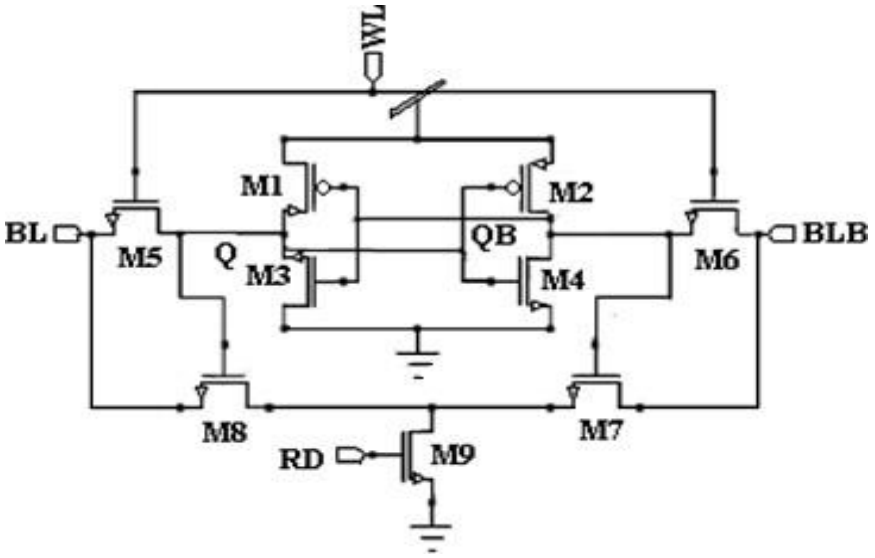


Fig 3.6: 9T SRAM

Write Operation:

In a 9T SRAM (Static Random Access Memory) cell, the write operation is performed by enabling the Write Word Line (WL) while keeping the Read Word Line (RWL) disabled and applying the Write Enable (WE) signal. This allows data to be written into the storage nodes without interfering with the read path, improving stability and reliability.

During the write operation, the access transistors MN5 and MN6 turn ON, allowing the data

from the bit-lines (BL and BLB) to be transferred into the cell. The storage nodes (Q and QB) are updated based on the bit-line values. If a ‘1’ is to be written, BL is set high (VDD) and BLB is set low (0V), whereas for a ‘0’, BL is low (0V) and BLB is high (VDD). The cross-coupled inverters (which store the data) switch states accordingly.

To minimize power consumption, transistor MN7 remains cut off during the write operation. This reduces leakage current in the read path, a technique known as Self-Controllable Current CMOS (SCCMOS). This approach ensures that only a small leakage current flows, improving energy efficiency and write stability. The 9T SRAM cell offers better write performance compared to a traditional 6T SRAM, as it reduces read disturbance and provides more stable operation, making it ideal for low-power and high-performance memory applications.

CHAPTER 4

SCHEMATIC DIAGRAM

4.1 6T SRAM CELL:

A 6T SRAM (Static Random Access Memory) cell is the most commonly used memory cell in modern processors and cache memory due to its balance of speed, power efficiency, and area utilization. It consists of six transistors: four transistors form two cross-coupled inverters that store data, while two NMOS transistors act as access transistors for read and write operations. This design ensures that the stored data remains stable as long as power is supplied.

During the write operation, the word line (WL) is enabled, allowing data to be written into the storage nodes via the bit-lines (BL and BLB). In the read operation, the word line activates the access transistors, allowing the stored value to influence the bit-lines, which are then sensed by a sense amplifier to determine the stored bit. However, since the same bit-lines are used for both reading and writing, the read operation can disturb the stored data, making the 6T SRAM less stable at lower voltages compared to higher-transistor SRAM designs.

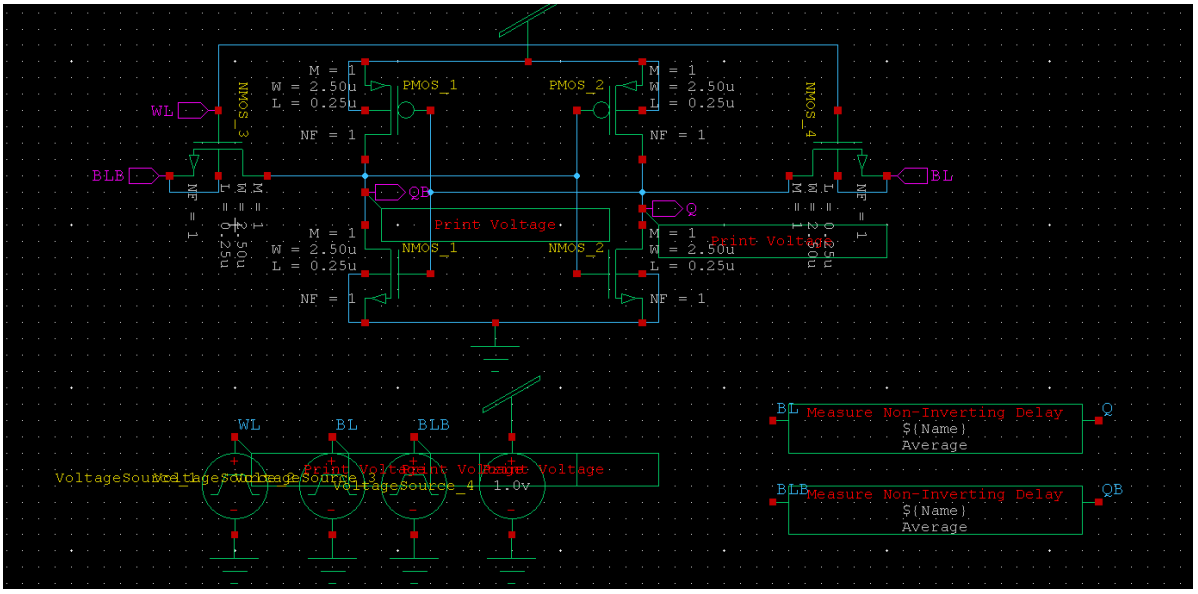


Fig 4.1: Schematic Diagram of 6T SRAM Cell

Despite this limitation, 6T SRAM is widely used due to its compact design, high speed, and lower power consumption compared to DRAM. It is commonly found in processor caches (L1, L2, L3), high-speed registers, and embedded memory in mobile and

computing devices. However, as technology advances and the demand for lower power and improved stability increases.

4.2 7T SRAM CELL

A 7T SRAM (Static Random Access Memory) cell is an advanced variation of the traditional 6T SRAM, designed to improve read stability and power efficiency. It consists of seven transistors: four transistors form two cross-coupled inverters for data storage, two NMOS transistors act as access transistors for read and write operations, and an additional seventh transistor is introduced to enhance read stability. In a standard 6T SRAM cell, the read operation can cause a disturbance in the stored data due to voltage fluctuations on the storage node. The extra transistor in 7T SRAM helps isolate the read operation from the storage nodes, preventing unwanted switching and reducing the risk of data corruption.

During a write operation, the word line (WL) is activated, allowing data to be written through the bit- lines. The stored data remains stable as long as power is supplied. In the read operation, instead of directly accessing the storage nodes, the additional transistor helps in selectively enabling the read path, thereby improving reliability and minimizing leakage currents. This design results in better noise margins, lower power consumption, and enhanced read stability, making it more suitable for low- power applications, embedded systems, and high-performance processors. However, compared to 6T SRAM, the 7T cell requires more area per memory cell, which can slightly increase fabrication costs..

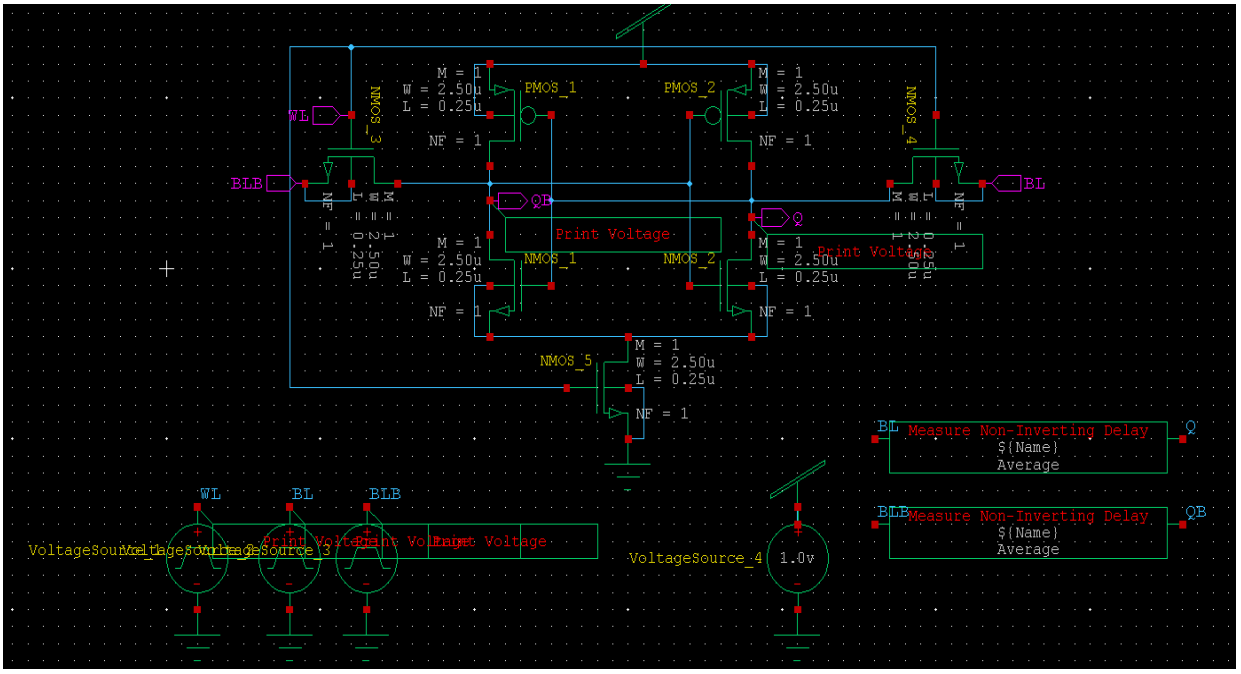


Fig 4.2: Schematic Diagram of 7T SRAM Cell

Write Operation

The write operation can be start by turning off the N5 transistor to this cut off feedback connection. When N3 is on and N4 is off the bit line bar carries complement of input data. The N5 is turned on and WL is turned off for reconnect the feedback connection to store new data. The bit line bar is discharged to “0” for storing “1” in the cell. And there is no need to discharge bit line for storing “0” in the cell.

Read Operation

When performing the read operation both read and word lines are turned to on and also the transistor N 5 is kept on.

4.3 8T SRAM CELL

An 8T SRAM (Static Random Access Memory) cell is designed to enhance read stability and reduce power consumption, making it ideal for low-power applications. It consists of eight transistors: four transistors form two cross-coupled inverters for data storage, two NMOS transistors function as write access transistors, and an additional two transistors are dedicated to a separate read buffer. This separation between the read and write paths significantly improves read stability, as the storage nodes are not directly accessed during the read operation, unlike in a traditional 6T SRAM. The read buffer ensures that the stored data remains undisturbed, preventing read disturbance issues commonly seen in 6T designs.

During a write operation, the word line (WL) is activated, allowing data to be stored through the bit- lines. In the read operation, the additional read access transistor and read bit-line enable a more reliable and low-power readout without affecting the storage node. This architecture eliminates read-induced failures, improves noise margins, and makes 8T SRAM a preferred choice for low-voltage and high- speed memory applications such as battery-operated devices, mobile processors, and IoT systems. However, the increased transistor counts results in a larger area per memory cell, making it less dense compared to 6T SRAM. Prior to write 1 at node Q, bit line is charged to VDD and write word line is pulled high. During write operation CS is maintained at 0v, to retain the stored content at node Q. During write ‘0’ the bit line is maintained at ground and signal CS at VDD, so that the charge stored at node Q can easily be inverted from 1 to 0. Which speed up the write operation and write ability of the proposed 8T SRAM cell.

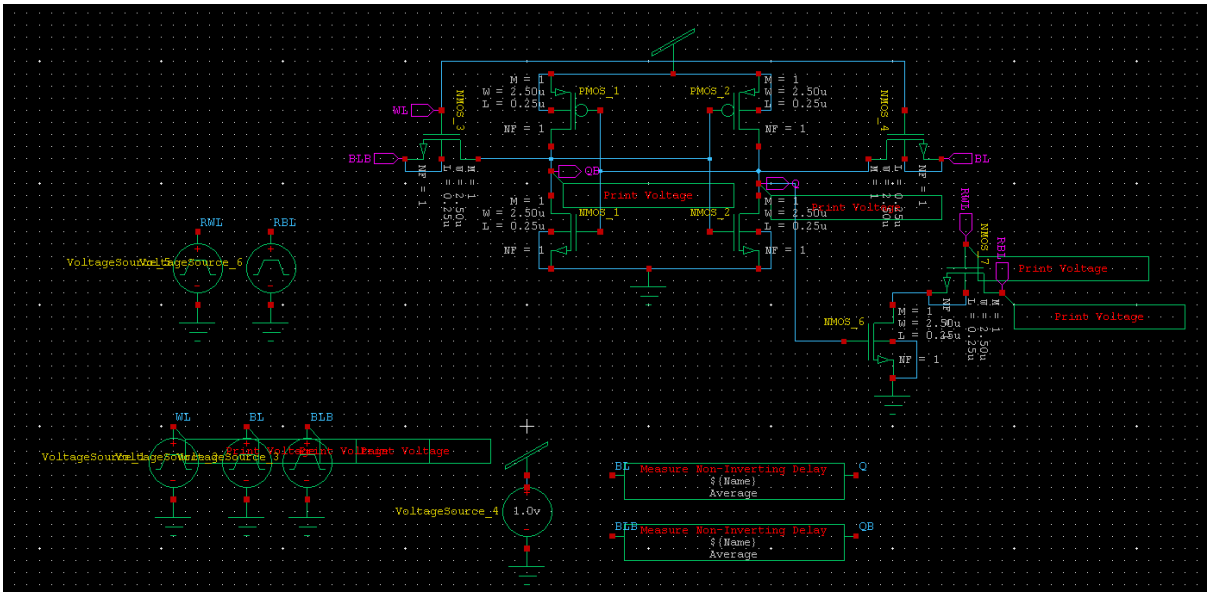


Fig 4.3: Schematic Diagram of 8T SRAM Cell

Before initiating the read operation, BL is kept at VDD while WWL and RWL are maintained at 0v and VDD respectively. In the proposed cell the storing node Q is directly connected to the PMOS (P_3) transistor. During read 1 operation P_3 gets turn off due to stored 1 at Q, RWL is activated. The pre-charged BL not get discharged due to turn off state of P_3, and 1 is read by sense amplifier. If '0' is stored at node Q, the connected PMOS gets turn on and when RWL is activated, the whole charged stored at BL is discharged through P_3 and N_5 and '0'is sensed by the sense amplifier.

4.4 9T SRAM CELL:

A 9T SRAM cell further improves power efficiency, read stability, and leakage current reduction by introducing a more complex transistor arrangement. It consists of nine transistors: four transistors form two cross-coupled inverters for data storage, two NMOS transistors handle write operations, and three additional transistors create a separate, fully isolated read path. The key advantage of the 9T SRAM design is that it completely eliminates read disturbance by ensuring that the storage nodes are not directly accessed during read operations.

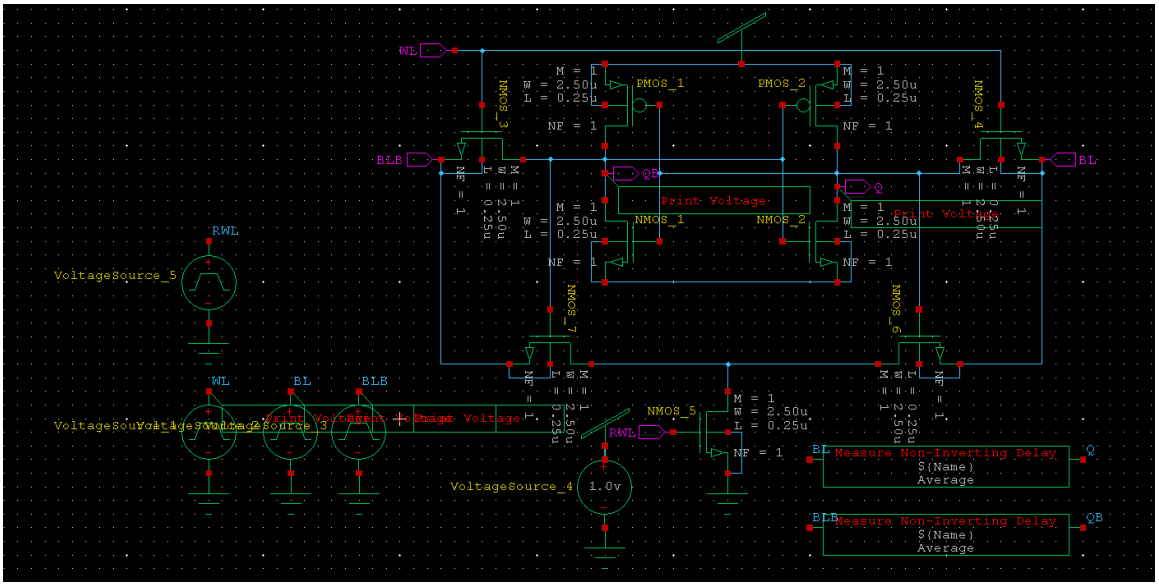


Fig 4.4: Schematic Diagram of 9T SRAM Cell

In the write operation, the word line (WL) is enabled, allowing data to be written into the storage nodes. For reading, a separate read bit-line and read word-line control the additional transistors, ensuring minimal power dissipation and improved read stability. The use of Self- Controllable Current CMOS (SCCMOS) techniques in some 9T designs helps in reducing leakage currents, making it ideal for low-power and ultra-low-voltage applications. The 9T architecture offers better performance, noise immunity, and lower power consumption, making it suitable for cache memories, embedded systems, and energy-efficient computing devices. However, similar to 8T SRAM, the higher transistor count increases the area per cell, making it slightly less area-efficient compared to 6T and 7T SRAM.

CHAPTER 5

RESULTS

6T SRAM CELL

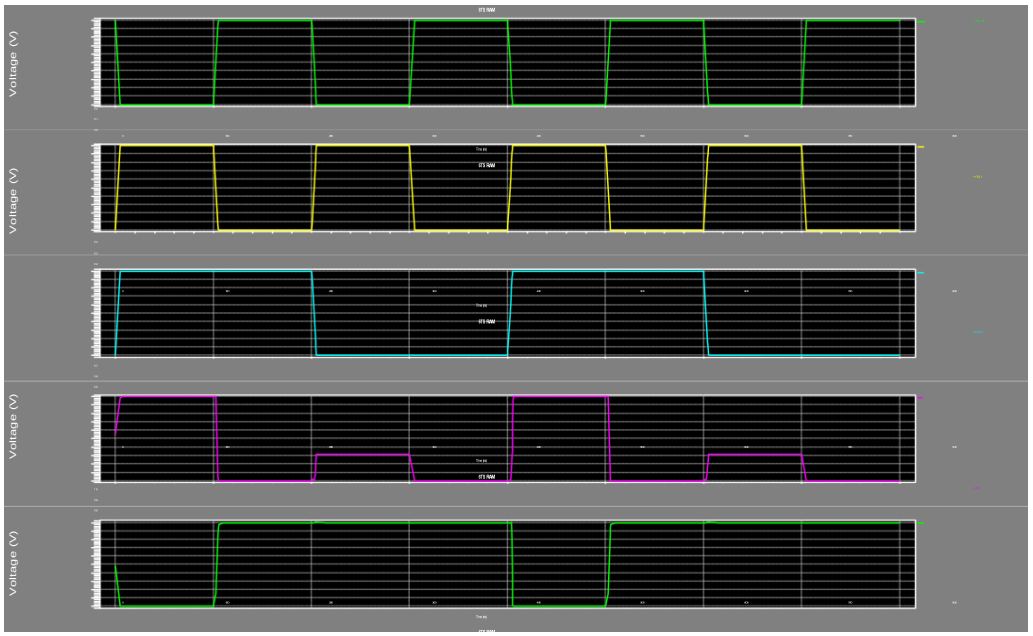


Fig 5.1: Simulation Result of 6T SRAM Cell

6t It has an average power consumption of 0.154 µW and a maximum power of 40.14 mW. Its read mode delay is 102.0 ns, while the write mode delay is 147.1 ps, making it suitable for balanced performance.

7T SRAM CELL

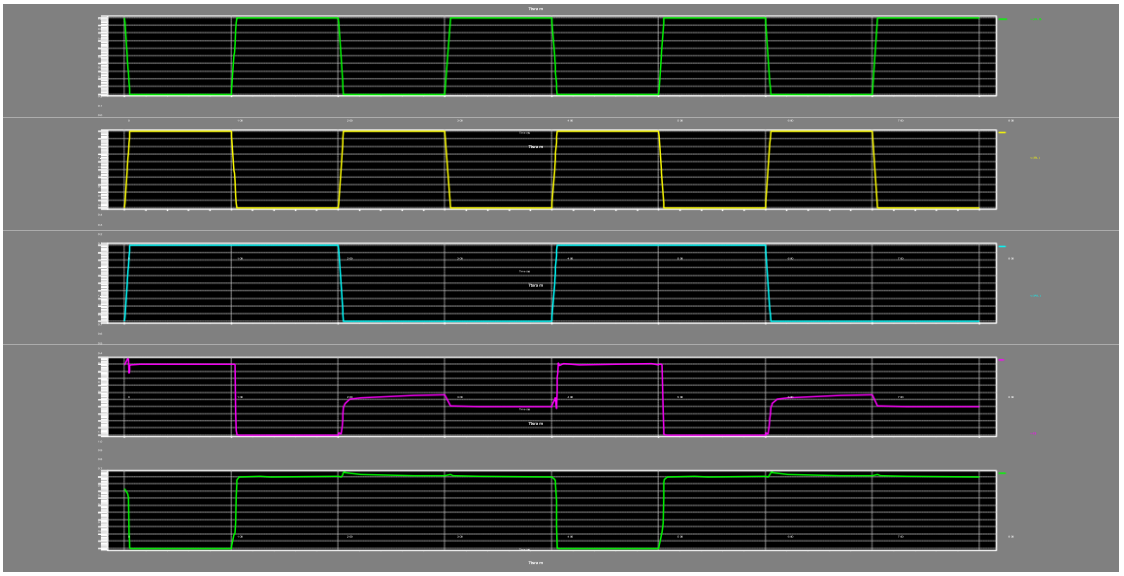


Fig 5.2: Simulation Result of 7T SRAM Cell

7T Transistor: Known for low average power (0.099 µW), it has a minimal power of 0.0016 nW. Its write mode delay is significantly high (1324.7 ps), indicating slower write operations compared to others.

8T SRAM CELL

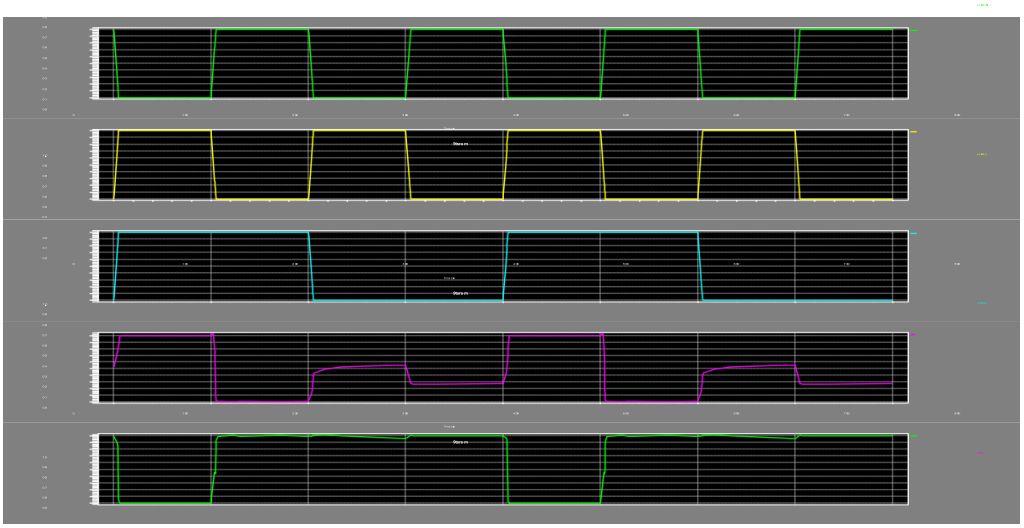


Fig 5.3: Simulation Result of 8T SRAM Cell

8T Transistor: With the highest average power (0.182 µW), it also features the highest maximum power (41.50 mW). It offers competitive delays with 102.0 ns (read) and 153.8 ps (write).

9T SRAM CELL

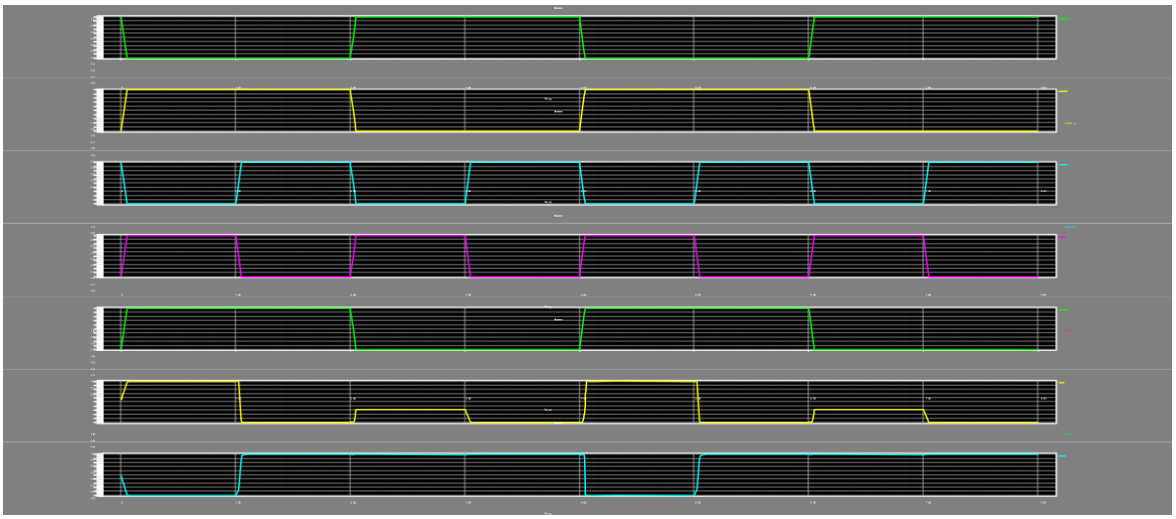


Fig 5.4: Simulation Result of 9T SRAM Cell

9T Transistor: Balances performance with moderate average power (0.135 µW) and maximum power (38.40 mW). Its write mode delay (827.7 ps) is better than the 7T, making it faster in write operations.

The performance evaluation metrics for the given 6T, 7T, 8T, and 9T SRAM cells based on the provided table are as follows:

1. Power Consumption Metrics

- Average Power (µW): Represents the mean power consumption of each SRAM cell type. The 7T cell consumes the least average power (0.099 µW), making it the most energy-efficient.
- Maximum Power (mW): Indicates the peak power consumption. The 7T SRAM has the lowest maximum power (34.91 mW), while 8T consumes the highest (41.50 mW).
- Minimum Power (nW): Represents the lowest power required during standby or low activity. The 7T cell shows the lowest minimum power consumption (0.0016 nW), indicating excellent leakage power control.

2. Speed and Delay Metrics

- Read Mode Delay (ns): Measures the time taken to read data from memory. All cells have a nearly identical read delay (~102 ns), with 7T and 9T showing a slight improvement (101.8 ns).
- Write Mode Delay (ps): Measures the time taken to write data into the memory cell. The 7T

Table 6.1: Comparison Of 6T,7T ,8T and 9T

Parameter	6T	7T	8T	9T
Avg. Power (µW)	0.154	0.099	0.182	0.135
Max Power (mW)	40.14	34.91	41.50	38.40
Min Power (nW)	19.52	0.0016	8.63	0.36
Read Mode Delay (ns)	102.0	101.8	102.0	101.8
Write Mode Delay (ps)	147.1	1324.7	153.8	827.7

ADVANTAGES

The project offers several notable advantages. Firstly, it provides a comprehensive understanding of various SRAM cell architectures—6T, 7T, 8T, and 9T—highlighting their respective trade-offs in terms of read/write stability, power consumption, and area efficiency. This allows for informed selection of memory topologies suitable for specific applications, especially at the 22nm technology node. By addressing design challenges at this scale, the project aligns with current semiconductor industry trends and supports optimization for low-power and high-performance applications. Notably, it emphasizes the relevance of 8T and 9T SRAM cells for low-power systems such as IoT devices and embedded platforms, where energy efficiency and data stability are critical.

The inclusion of 7T SRAM analysis offers insights into balancing performance and area, making it ideal for mid-range applications. Additionally, the project promotes improved memory reliability through the assessment of static noise margins and read/write decoupling strategies, which are crucial for mission-critical and high-reliability systems. Overall, the study not only aids in current SRAM design decisions but also lays a foundation for future research and development at more advanced nodes, making it valuable for both academic exploration and industrial implementation.

APPLICATIONS

This project has broad applications in both academic research and industry, particularly in the design and optimization of memory systems for advanced integrated circuits. One of the key application areas is in low-power electronic devices, such as Internet of Things (IoT) sensors, wearables, and battery-powered systems, where SRAM cells like 8T and 9T are favored for their enhanced stability and low leakage power. In high-performance computing and general-purpose processors, the compact and fast 6T and 7T cells are suitable due to their area efficiency and speed, making them ideal for use in cache memories. Additionally, the findings of this project are useful in mission-critical applications, such as automotive, aerospace, and medical electronics, where memory reliability is crucial and stability-enhanced cells like 9T are preferable. Furthermore, the project is applicable in academic settings, offering foundational knowledge for students and researchers working in VLSI design, embedded systems, and semiconductor technology scaling. By providing design insights across multiple SRAM architectures, the project helps guide efficient memory integration in a wide range of modern and emerging electronic systems.

CHAPTER – 6
CONCLUSION AND FUTURE SCOPE

CONCLUSION

The conclusion of the performance evaluation and comparison of 4T, 6T, 7T, 8T, and 9T SRAM at the 22nm technology node provides valuable insights into the characteristics and suitability of each SRAM cell design. the choice of SRAM cell design should be based on a thorough understanding of the application's requirements and trade-offs. While lower-transistor-count designs like the 6T SRAM cells may offer advantages in terms of area and speed, higher-transistor- count designs like the 9T SRAM cell provide enhanced stability and reliability, albeit at the cost of increased power consumption and area.

In Future may focus on further optimizing SRAM cell designs to achieve a balance between performance, power efficiency, and area occupancy in advanced technology nodes. Optimization of SRAM cell structures to achieve a better trade-off between power consumption, performance, and area utilization, particularly as technology nodes continue to scale down. Advanced techniques such as FinFET-based SRAM, near-threshold computing, and hybrid memory architectures could play a key role in enhancing next-generation SRAM designs for emerging applications like IoT, AI Accelerator.

FUTURE SCOPE

As technology continues to scale down, evaluating SRAM cell performance at the 22nm node and beyond presents several opportunities for innovation in power efficiency, stability, and reliability. One significant area of future research is the adoption of FinFET and Gate-All-Around (GAA) FET-based SRAM designs, as bulk CMOS technology faces scaling challenges. These advanced transistor architectures can be analyzed for their impact on read/write stability, leakage power, and overall performance in different SRAM topologies. Additionally, with the growing demand for low-power applications such as IoT, wearable devices, and AI accelerators, future studies can focus on ultra-low voltage SRAM cells optimized for near-threshold and sub-threshold operation, incorporating techniques like adaptive body biasing and power gating to minimize energy consumption.

Another key area of exploration is the integration of non-volatile memory technologies such as Resistive RAM (RRAM), Magnetic RAM (MRAM), and Ferroelectric FET (FeFET) SRAM, which can enhance data retention and reduce standby power without compromising speed.

Furthermore, as technology nodes shrink, soft errors and process variations become more prominent, necessitating the development of error-resilient SRAM architectures with built-in Error Correction Code (ECC) mechanisms and radiation-hardened designs for mission-critical applications in space, automotive, and defense industries. Future research may also focus on machine learning-based optimization techniques to dynamically adjust SRAM performance, power, and stability based on real-time workload requirements. By addressing these challenges and leveraging emerging memory technologies, SRAM designs at advanced nodes can achieve a better balance between power efficiency, performance, and reliability, paving the way for next-generation computing architectures.

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APPENDEX

S-Edit (Schematic Editor)

S-Edit is the schematic capture tool in the Tanner EDA tool suite, serving as the essential first step in the analog and mixed-signal IC design process. It provides a user-friendly graphical interface for drawing, editing, and managing circuit schematics, enabling designers to efficiently model circuit behavior before moving on to simulation or physical implementation. S-Edit supports both flat and hierarchical schematic entry, which is beneficial for managing large and complex designs. Its drag-and-drop interface, coupled with customizable component libraries, allows for easy creation and reuse of circuit elements. S-Edit allows automatic generation of netlists that are compatible with SPICE simulators, especially T-Spice, making it simple to transition from schematic to simulation.

The tool also features Design Rule Check (DRC) and Electrical Rule Check (ERC) to help detect errors such as floating nodes, unconnected pins, or short circuits early in the design process. These features help prevent costly mistakes during layout and fabrication. S-Edit supports behavioral modeling using Verilog-A, enabling high-level abstraction and faster simulation. Furthermore, S-Edit allows for seamless integration with L-Edit, enabling back-annotation and layout-driven schematic updates. This bidirectional link ensures design consistency throughout the development cycle. S-Edit also provides features like property editing, signal naming, annotation tools, and variant management for design reuse across different projects or process nodes.

The interface allows for easy zooming, panning, and component highlighting, improving user efficiency and schematic readability. This tool is especially popular in academia due to its simplicity, but it also provides the advanced capabilities needed for commercial circuit design. Whether designing small analog blocks or complex system-level circuits, S-Edit supports every stage of schematic development with flexibility and precision. With robust simulation compatibility, hierarchical design support, and a powerful graphical interface, S-Edit forms the foundation of Tanner's integrated design flow, offering the functionality and ease of use that engineers and students alike require for schematic-based design. With intuitive drag-and-drop features, parameter editing, and hierarchical instantiation, it significantly simplifies schematic creation and modification. Furthermore, it allows efficient management of circuit variants, reuse of design blocks, and easy adaptation to new process nodes. Overall, it serves as a critical tool for rapid prototyping, academic learning, and professional schematic-based circuit design.

L-Edit (Layout Editor)

L-Edit is the layout design tool in the Tanner EDA suite, specifically developed for creating full-custom layouts of analog, mixed-signal, and MEMS integrated circuits. It enables the physical implementation of circuits designed in S-Edit by providing a robust environment for drawing transistor-level layouts using polygons, paths, and predefined cells. L-Edit supports industry-standard file formats such as GDSII and OASIS, ensuring compatibility with foundry processes and other EDA tools. It provides a grid-based editor with powerful drawing and editing features, including parameterized cells (PCells), which allow for efficient design reuse and consistent layout generation.

One of the standout features of L-Edit is its integration with design rule checking (DRC) and layout versus schematic (LVS) tools, enabling users to validate their physical layout against foundry rules and the original schematic. This ensures correctness before tape-out. The tool also supports parasitic extraction and electrical rule checking, enhancing post-layout simulation accuracy. L-Edit's scripting support and customization options allow advanced users to automate repetitive tasks, increasing productivity and reducing human error. The graphical interface is optimized for large designs and provides multiple layers of zoom and object management for detailed work on dense layouts.

L-Edit is widely used in educational environments due to its simplicity and effectiveness, but it is also robust enough for professional use in commercial tape-outs. It allows for precise control of geometry, metal layers, and via placements, which are critical in analog and MEMS applications. With its tight integration with S-Edit and W-Edit, L-Edit supports an efficient design flow from schematic to layout to simulation. Overall, L-Edit is a highly capable layout editor that balances usability with advanced functionality, making it a preferred choice for designers working on low- to medium-complexity IC layouts.

The layout editor features multiple editing layers, zoom tools, snap-to-grid functionality, and color-coded layer representation, making the layout process more intuitive and manageable. L-Edit is especially effective for analog and MEMS design due to its support for irregular geometries and precision editing. It also enables hierarchical layout, allowing complex systems to be built from smaller, reusable blocks. The tool’s efficiency, performance, and intuitive interface make it a preferred choice in educational and industrial environments alike. L-Edit plays a central role in closing the design loop by bridging the schematic and simulation stages with fabrication-ready layout design, forming an integral part of the Tanner design ecosystem.

W-Edit (Waveform Viewer)

W-Edit is the waveform analysis tool in the Tanner EDA suite, designed to visualize and analyze simulation results produced by T-Spice and other compatible SPICE simulators. It serves as the final step in the IC design and verification workflow, providing detailed insights into the time-domain behavior of electrical signals in a circuit. W-Edit allows users to view voltage, current, power, and other simulation outputs over time with high precision and interactivity. The tool supports multiple data formats, such as .tr0, .raw, and .csv, making it highly flexible for various simulation environments. Engineers can load simulation results and graphically analyze them using cursors, zoom, and pan tools.

With the help of measurement cursors, users can extract critical timing parameters such as rise time, fall time, propagation delay, and overshoot directly from waveforms. It also offers advanced mathematical functions for waveform processing, allowing users to compute differences, perform signal transformations, or generate derived waveforms. One of W-Edit's key strengths lies in its seamless integration with S-Edit and T-Spice, which streamlines the process of moving from schematic to simulation to analysis without switching platforms. Users can instantly launch simulations from S-Edit and view results in W-Edit, greatly improving design efficiency.

W-Edit also supports multi-window viewing, which is useful when comparing different signals or verifying functionality across various simulation runs. It allows engineers to overlay waveforms, synchronize time axes, and annotate graphs, making it easier to document and present simulation outcomes. The interface is designed to be both powerful and accessible, making it suitable for academic use as well as professional circuit debugging. W-Edit is especially valuable in analog and mixed-signal design, where visualizing continuous-time behavior is crucial for understanding circuit performance. In combination with S-Edit and L-Edit, W-Edit completes the Tanner toolchain, offering a comprehensive and user-friendly environment for IC design, simulation, and verification.